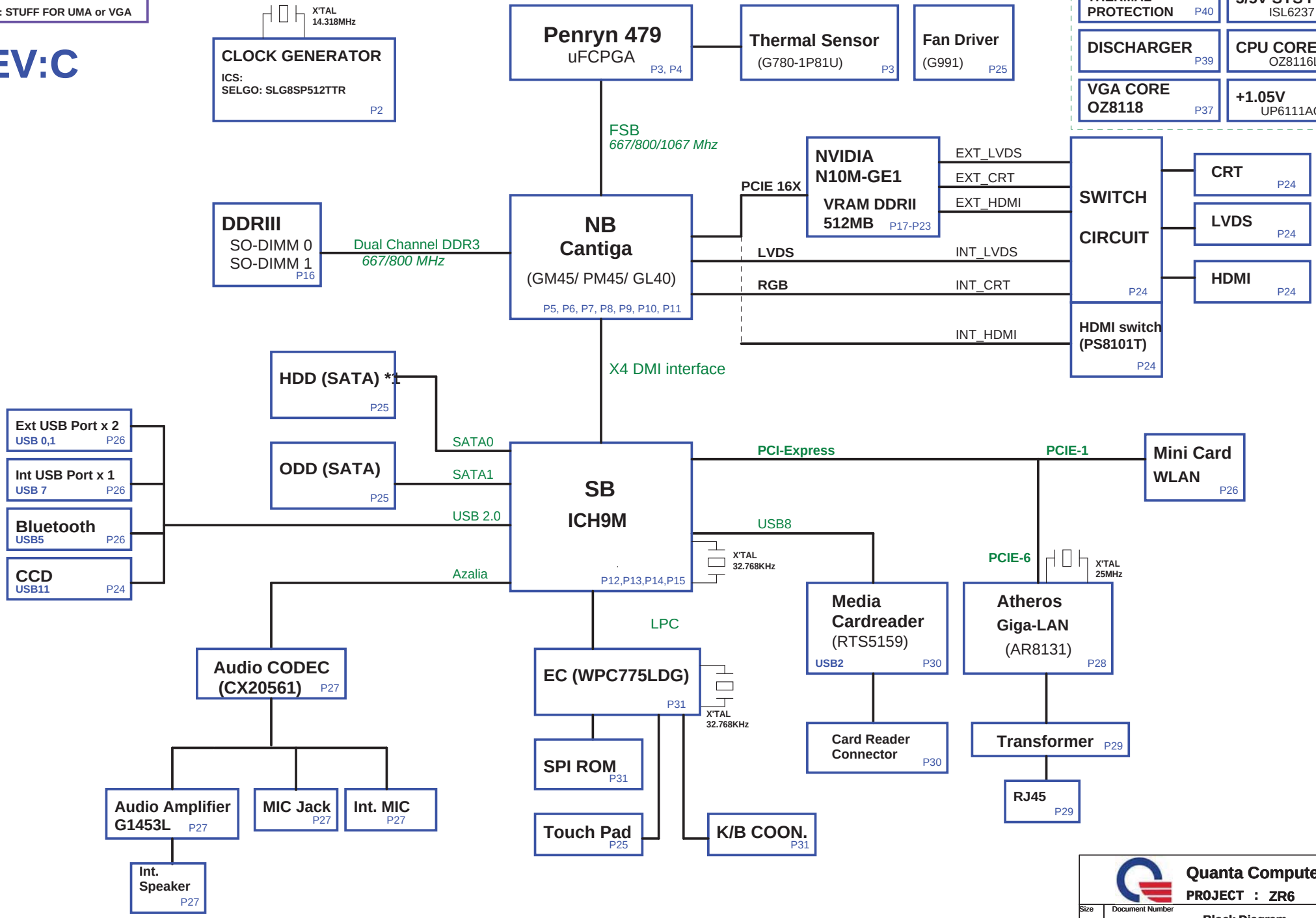
ZR6 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:C



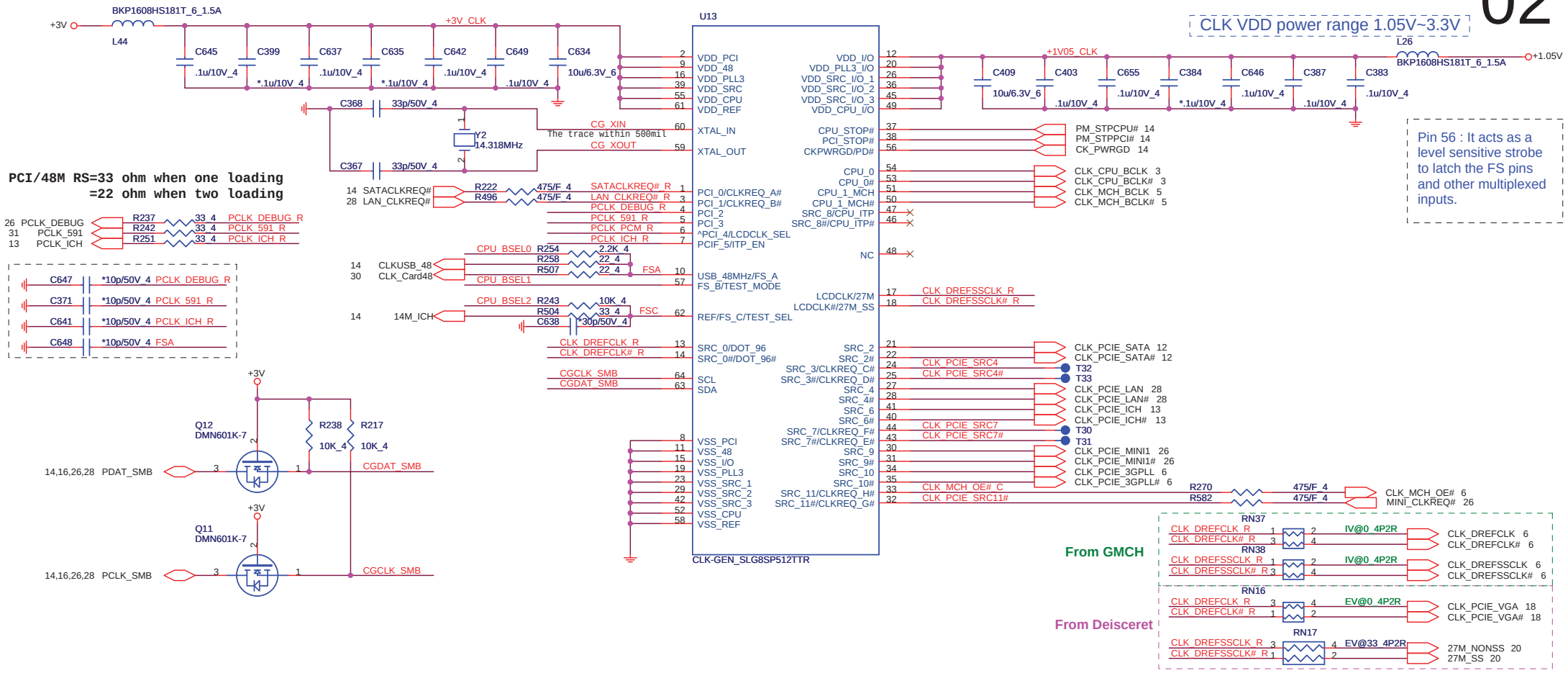
Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, April 13, 2009 Sheet 1 of 42

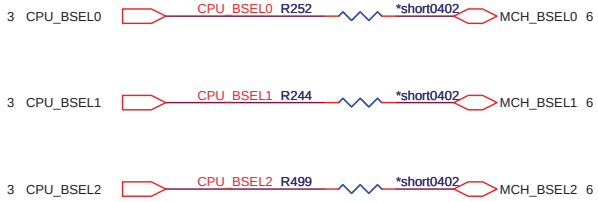
Clock Generator (CLK)

02



CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



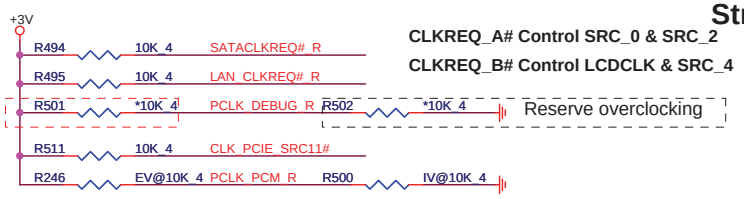
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

CLKREQ_A# Control SRC_0 & SRC_2

CLKREQ_B# Control LCDCLK & SRC_4



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

PCLK_ICH_R R503 10K_4

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLOCK GENERATOR

Quanta Computer Inc.

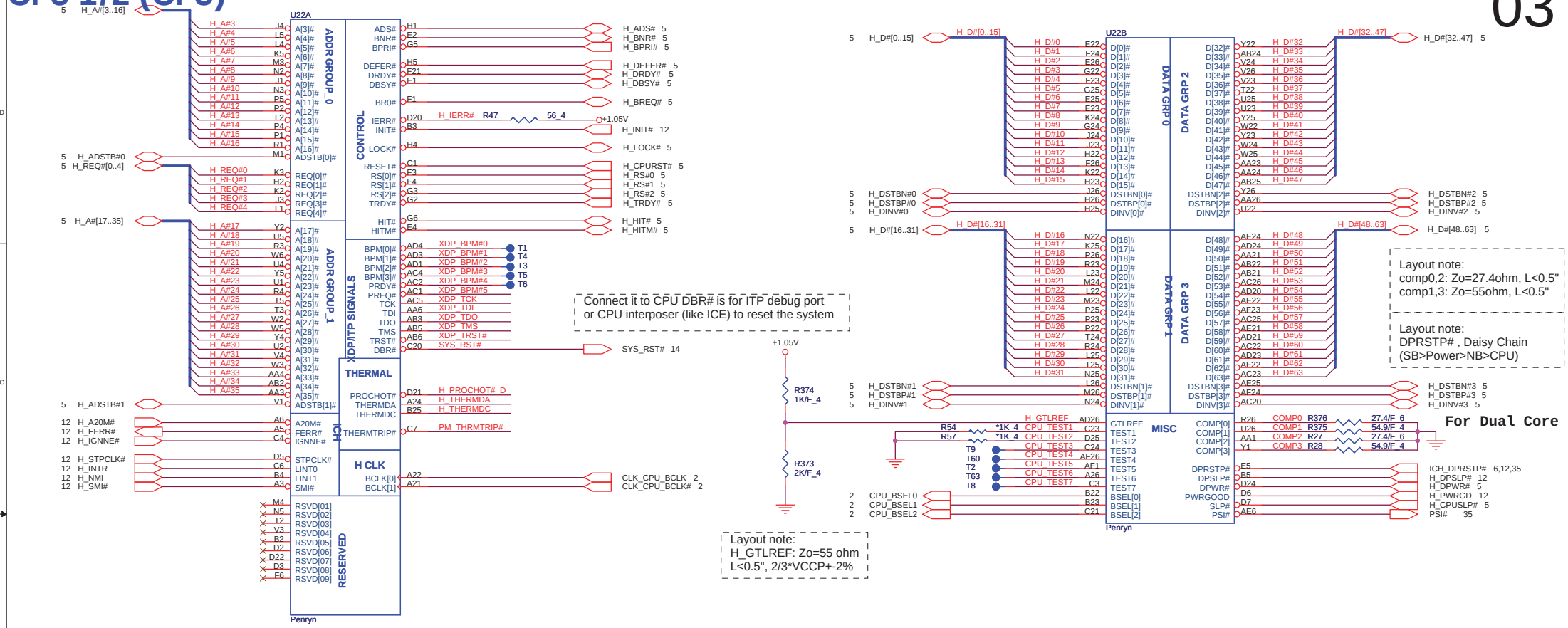
PROJECT : ZR6

Size	Document Number	Rev
	CLOCK GENERATOR	1A

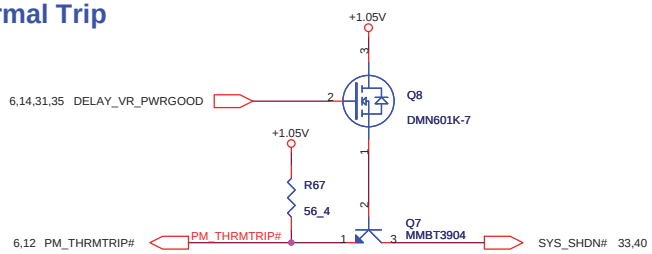
Date: Monday, April 13, 2009 Sheet 2 of 42

CPU 1/2 (CPU)

03



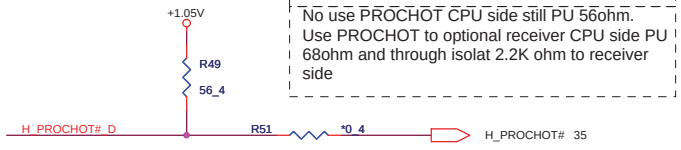
Thermal Trip



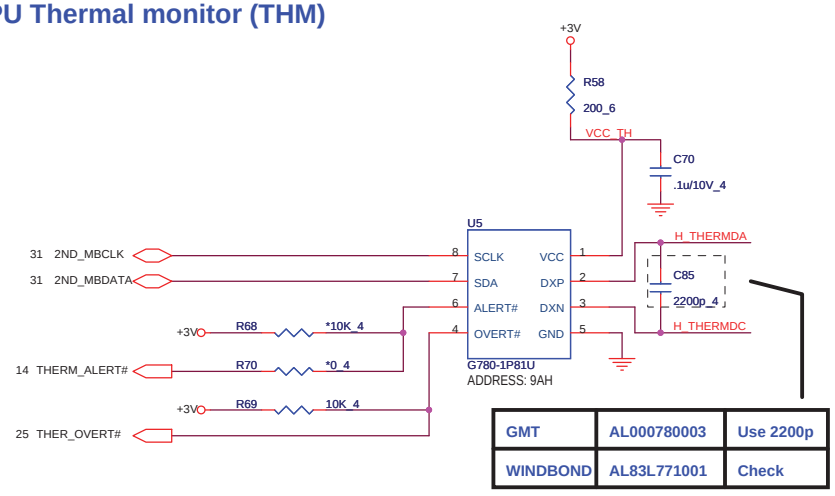
Processor hot

No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

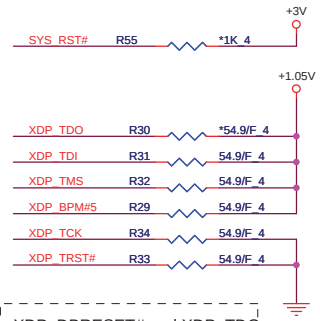


CPU Thermal monitor (THM)



GMT	AL000780003	Use 2200p
WINDBOND	AL83L771001	Check

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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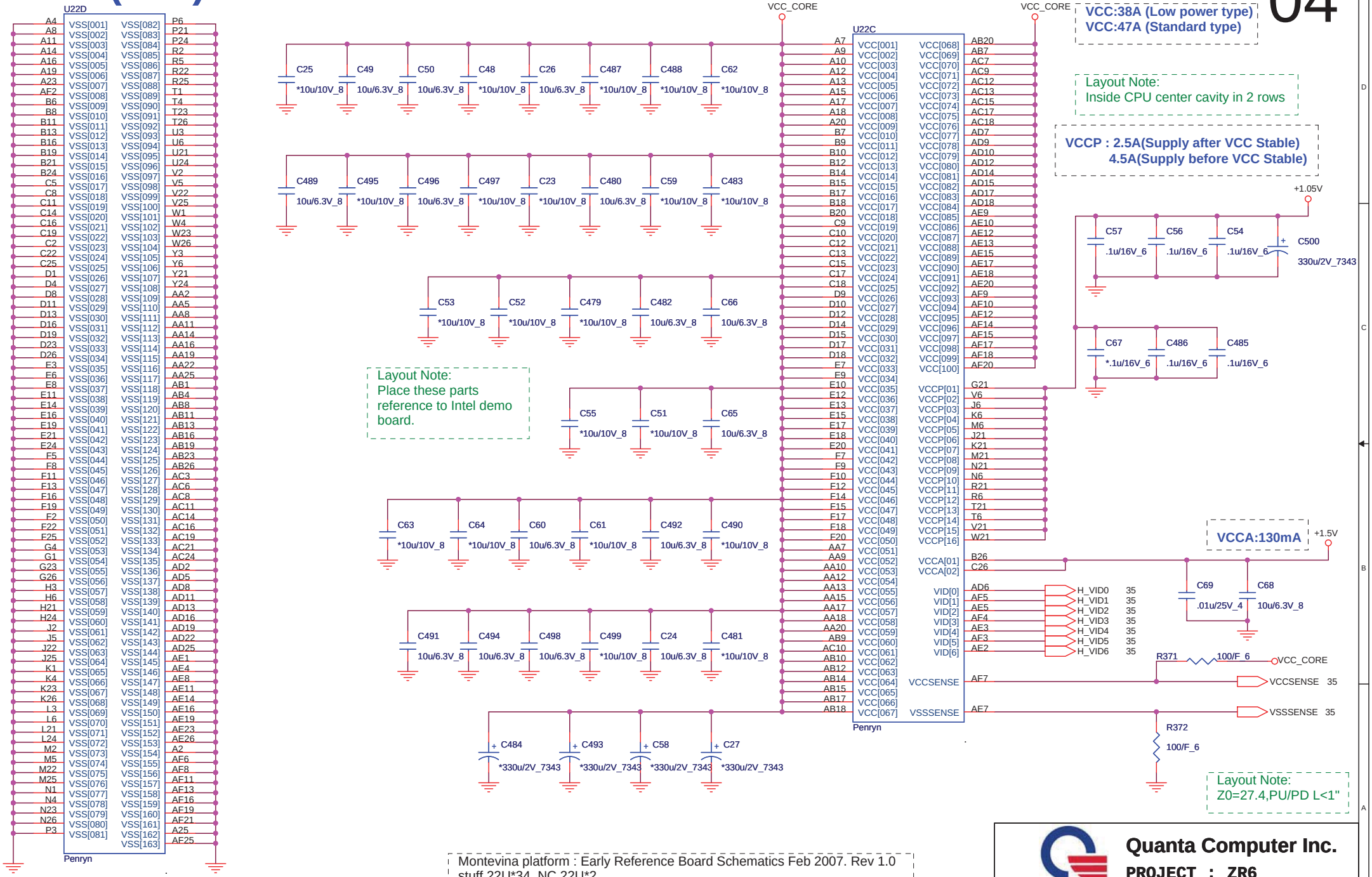
PROJECT : ZR6

Size	Document Number	Rev
	CPU Host Bus	1A

Date: Monday, April 13, 2009 Sheet 3 of 42

CPU 2/2 (CPU)

04



Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	CPU Power	1A

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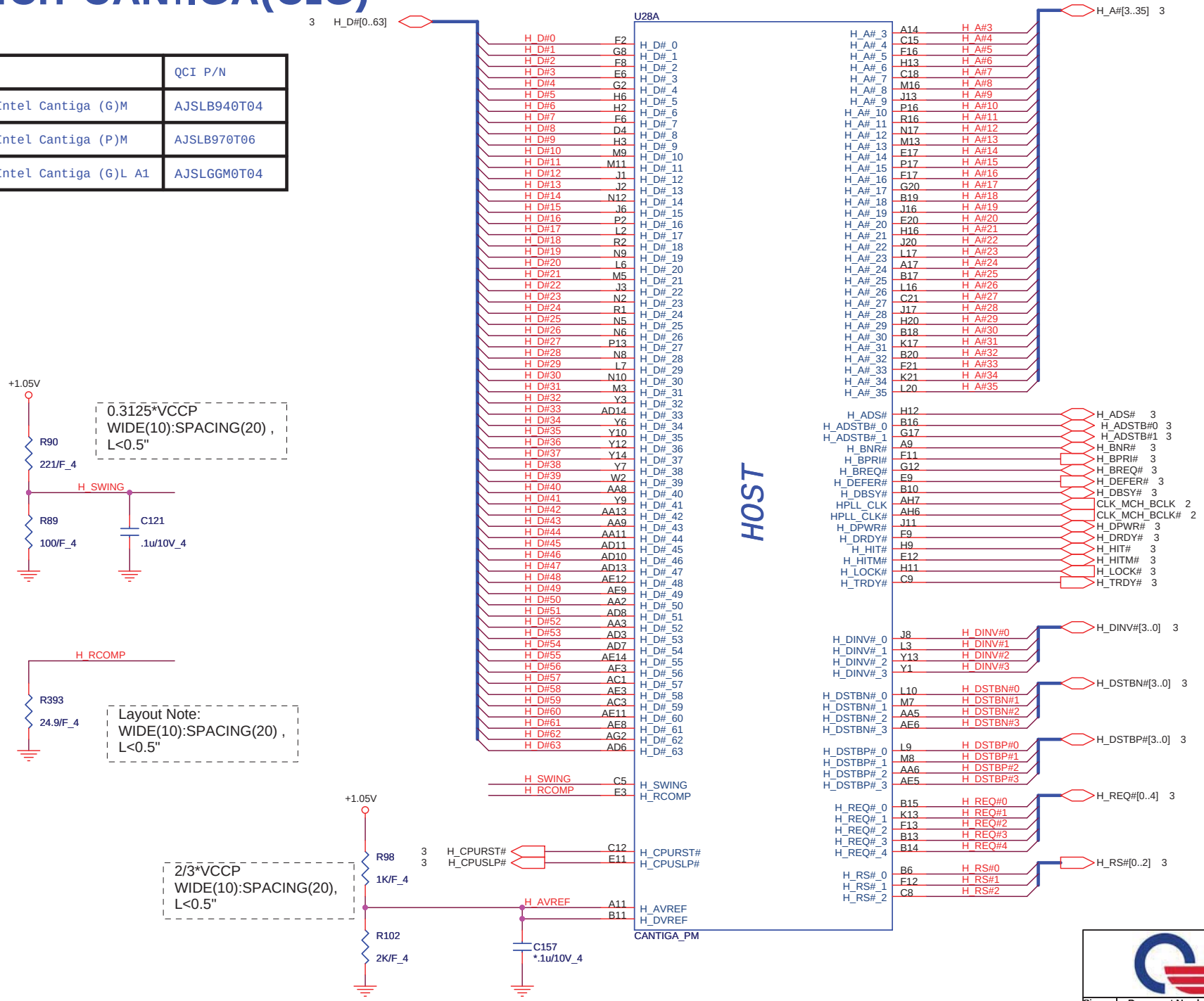
GMCH-CANTIGA(CLG)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	GMCH HOST	1A

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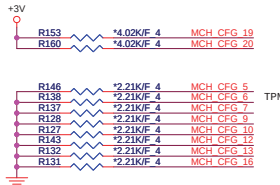
GMCH-CANTIGA(CLG)

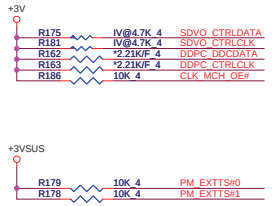
IV@
EV@

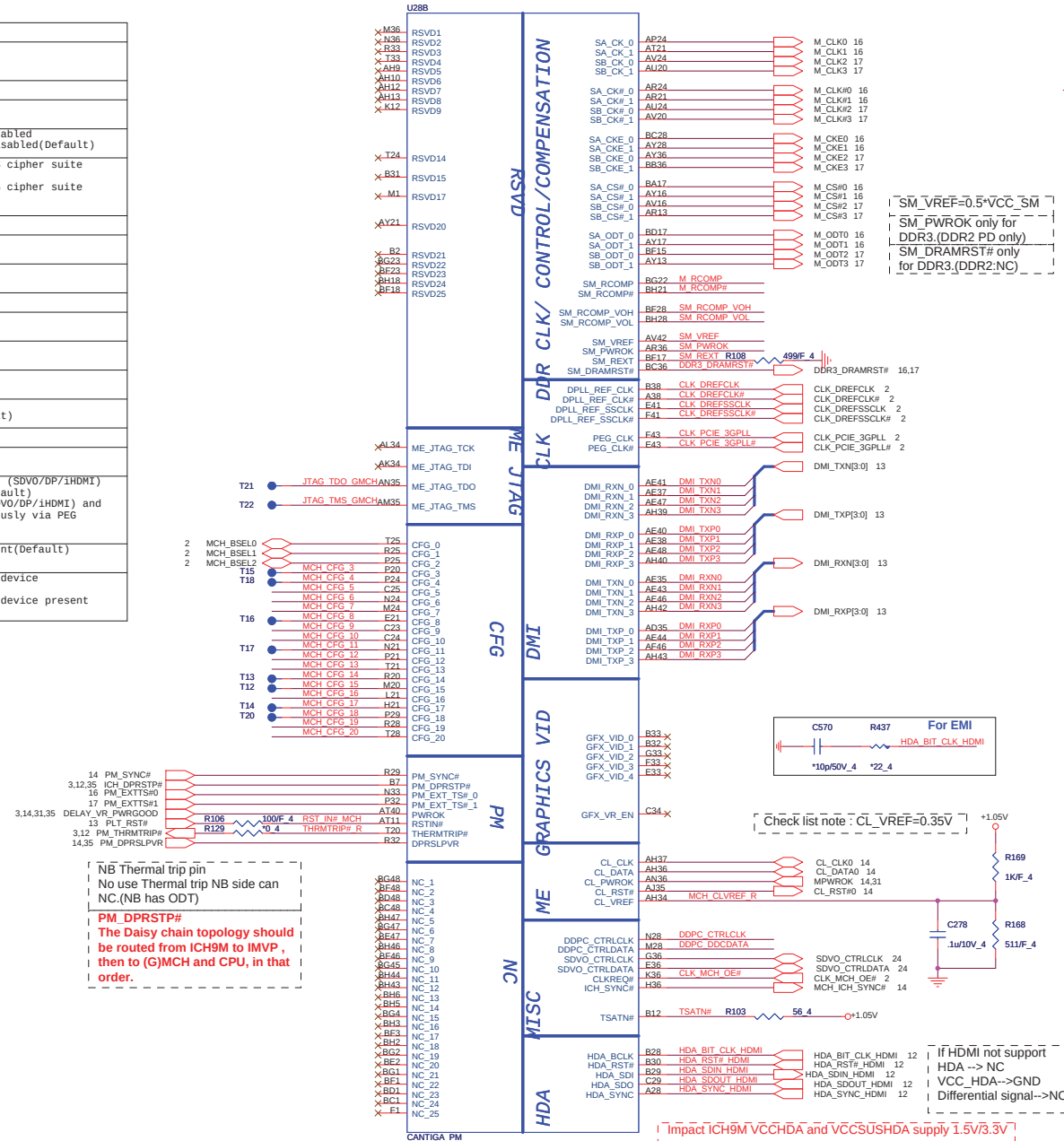
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ mode	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin







Quanta Computer Inc.
PROJECT : ZR6
Size | Document Number | Rev
GMCH DMI | 1A
Date: Monday, April 13, 2009 Sheet 6 of 42

GMCH-CANTIGA(CLG)

IV@
EV@
SP@

IV&EV Dis/Enable setting
If LVDS no use,all signal can NC

U28C

24 L_BKLT_CTRL — L32 L_BKLT_CTRL
24 INT_LVDS_BLON — G32 L_BKLT_EN
R171 IV@10K_4 L_CTRL_CLK — M32 L_CTRL_CLK
+3V — R172 IV@10K_4 L_CTRL_DATA — M33 L_CTRL_DATA
24 INT_LVDS_EDIDCLK — K33 L_DDC_CLK
24 INT_LVDS_EDIDDATA — J33 L_DDC_DATA
24 INT_LVDS_DIGON — M29 L_VDD_EN
R195 IV@2.4K/F_4 LVDS_IBG — C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
24 INT_TXLCLKOUT- — INT_TXLCLKOUT- — C41 LVDSA_CLK#
24 INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — C40 LVDSA_CLK
B37 LVDSB_CLK#
A37 LVDSB_CLK
24 INT_TXLOUT0- — INT_TXLOUT0- — H47 LVDSA_DATA#_0
24 INT_TXLOUT1- — INT_TXLOUT1- — E46 LVDSA_DATA#_1
24 INT_TXLOUT2- — INT_TXLOUT2- — G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
24 INT_TXLOUT0+ — INT_TXLOUT0+ — H48 LVDSA_DATA_0
24 INT_TXLOUT1+ — INT_TXLOUT1+ — D45 LVDSA_DATA_1
24 INT_TXLOUT2+ — INT_TXLOUT2+ — F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
A41 LVDSB_DATA#_0
H38 LVDSB_DATA#_1
G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
B42 LVDSB_DATA_0
G38 LVDSB_DATA_1
F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm
R147 SP@75_4 INT_TV_COMP — F25 TVA_DAC
R136 SP@75_4 INT_TV_Y/G — H25 TVB_DAC
R151 SP@75_4 INT_TV_C/R — K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TV

24 INT_CRT_BLU — INT_CRT_BLU — E28 CRT_BLUE
24 INT_CRT_GRN — INT_CRT_GRN — G28 CRT_GREEN
24 INT_CRT_RED — INT_CRT_RED — J28 CRT_RED
G29 CRT_IRTN
24 INT_CRT_DDCCLK — H32 CRT_DDC_CLK
24 INT_CRT_DDCDAT — J32 CRT_DDC_DATA
24 INT_HSYNC — R158 IV@30.1_4 HSYNC_G — J29 CRT_HSYNC
CRTIREF — E29 CRT_TVO_IREF
24 INT_VSYNC — R165 IV@30.1_4 VSYNC_G — L29 CRT_VSYNC

VGA

HSYNC/VSYNC serial R place close to NB

CANTIGA_PM

GRAPHICS

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

PEG_COMPI — T37 EXP_A_COMPX — R176 49.9/F_4
PEG_COMPO — T36

PEG_RX#_0 — H44 PEG_RXN0
PEG_RX#_1 — J46 PEG_RXN1
PEG_RX#_2 — L44 PEG_RXN2
PEG_RX#_3 — L40 PEG_RXN3
PEG_RX#_4 — N41 PEG_RXN4
PEG_RX#_5 — P48 PEG_RXN5
PEG_RX#_6 — N44 PEG_RXN6
PEG_RX#_7 — T43 PEG_RXN7
PEG_RX#_8 — U43 PEG_RXN8
PEG_RX#_9 — Y43 PEG_RXN9
PEG_RX#_10 — Y48 PEG_RXN10
PEG_RX#_11 — Y36 PEG_RXN11
PEG_RX#_12 — AA43 PEG_RXN12
PEG_RX#_13 — AD37 PEG_RXN13
PEG_RX#_14 — AC47 PEG_RXN14
PEG_RX#_15 — AD39 PEG_RXN15 — PEG_RXN[15:0] 18

PEG_RX_0 — H43 PEG_RXP0
PEG_RX_1 — J44 PEG_RXP1
PEG_RX_2 — L43 PEG_RXP2
PEG_RX_3 — L41 PEG_RXP3
PEG_RX_4 — N40 PEG_RXP4
PEG_RX_5 — P47 PEG_RXP5
PEG_RX_6 — N43 PEG_RXP6
PEG_RX_7 — T42 PEG_RXP7
PEG_RX_8 — U42 PEG_RXP8
PEG_RX_9 — Y42 PEG_RXP9
PEG_RX_10 — W47 PEG_RXP10
PEG_RX_11 — Y37 PEG_RXP11
PEG_RX_12 — AA42 PEG_RXP12
PEG_RX_13 — AD36 PEG_RXP13
PEG_RX_14 — AC48 PEG_RXP14
PEG_RX_15 — AD40 PEG_RXP15 — PEG_RXP[15:0] 18,24

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PCI-EXPRESS

PEG_TX#_0 — J41 C_PEG_TXN0 C583 — .1u/10V_4 PEG_TXN0
PEG_TX#_1 — M46 C_PEG_TXN1 C587 — .1u/10V_4 PEG_TXN1
PEG_TX#_2 — M47 C_PEG_TXN2 C591 — .1u/10V_4 PEG_TXN2
PEG_TX#_3 — M40 C_PEG_TXN3 C596 — .1u/10V_4 PEG_TXN3
PEG_TX#_4 — M42 C_PEG_TXN4 C618 — EV@.1U/10V_4 PEG_TXN4
PEG_TX#_5 — R48 C_PEG_TXN5 C588 — EV@.1U/10V_4 PEG_TXN5
PEG_TX#_6 — N38 C_PEG_TXN6 C600 — EV@.1U/10V_4 PEG_TXN6
PEG_TX#_7 — T40 C_PEG_TXN7 C598 — EV@.1U/10V_4 PEG_TXN7
PEG_TX#_8 — U37 C_PEG_TXN8 C604 — EV@.1U/10V_4 PEG_TXN8
PEG_TX#_9 — U40 C_PEG_TXN9 C603 — EV@.1U/10V_4 PEG_TXN9
PEG_TX#_10 — Y40 C_PEG_TXN10 C608 — EV@.1U/10V_4 PEG_TXN10
PEG_TX#_11 — AA46 C_PEG_TXN11 C594 — EV@.1U/10V_4 PEG_TXN11
PEG_TX#_12 — AA37 C_PEG_TXN12 C616 — EV@.1U/10V_4 PEG_TXN12
PEG_TX#_13 — AA40 C_PEG_TXN13 C619 — EV@.1U/10V_4 PEG_TXN13
PEG_TX#_14 — AD43 C_PEG_TXN14 C614 — EV@.1U/10V_4 PEG_TXN14
PEG_TX#_15 — AC46 C_PEG_TXN15 C593 — EV@.1U/10V_4 PEG_TXN15 — PEG_TXN[15:0] 18,24

PEG_TX_0 — J42 C_PEG_TXP0 C580 — .1u/10V_4 PEG_TXP0
PEG_TX_1 — L46 C_PEG_TXP1 C585 — .1u/10V_4 PEG_TXP1
PEG_TX_2 — M48 C_PEG_TXP2 C590 — .1u/10V_4 PEG_TXP2
PEG_TX_3 — M39 C_PEG_TXP3 C597 — .1u/10V_4 PEG_TXP3
PEG_TX_4 — M43 C_PEG_TXP4 C611 — EV@.1U/10V_4 PEG_TXP4
PEG_TX_5 — R47 C_PEG_TXP5 C586 — EV@.1U/10V_4 PEG_TXP5
PEG_TX_6 — N37 C_PEG_TXP6 C601 — EV@.1U/10V_4 PEG_TXP6
PEG_TX_7 — T39 C_PEG_TXP7 C599 — EV@.1U/10V_4 PEG_TXP7
PEG_TX_8 — U36 C_PEG_TXP8 C605 — EV@.1U/10V_4 PEG_TXP8
PEG_TX_9 — U39 C_PEG_TXP9 C602 — EV@.1U/10V_4 PEG_TXP9
PEG_TX_10 — Y39 C_PEG_TXP10 C609 — EV@.1U/10V_4 PEG_TXP10
PEG_TX_11 — Y46 C_PEG_TXP11 C595 — EV@.1U/10V_4 PEG_TXP11
PEG_TX_12 — AA36 C_PEG_TXP12 C617 — EV@.1U/10V_4 PEG_TXP12
PEG_TX_13 — AA39 C_PEG_TXP13 C620 — EV@.1U/10V_4 PEG_TXP13
PEG_TX_14 — AD42 C_PEG_TXP14 C615 — EV@.1U/10V_4 PEG_TXP14
PEG_TX_15 — AD46 C_PEG_TXP15 C592 — EV@.1U/10V_4 PEG_TXP15 — PEG_TXP[15:0] 18,24

IV&EV Dis/Enable setting
<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm
R161 SP@1K/F_4 CRTIREF

SP@
CRT_R/G/B
For IV: 150ohm
For EV:0ohm
R155 SP@150/F_4 INT_CRT_BLU
R154 SP@150/F_4 INT_CRT_GRN
R150 SP@150/F_4 INT_CRT_RED

Discrete Stuffed. (CRT)
HSYNC_G
VSYNC_G
R159 EV@0_4
R166 EV@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	GMCH VGA	1A

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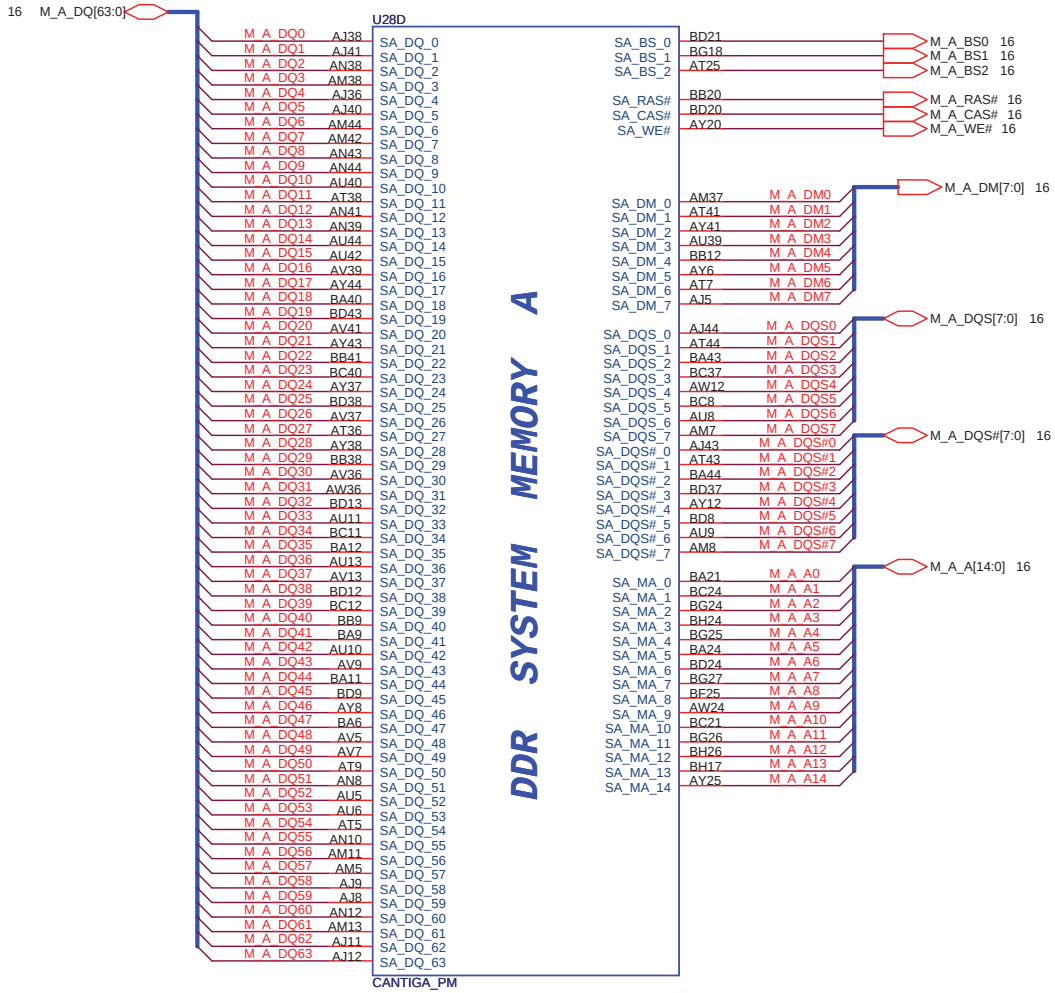
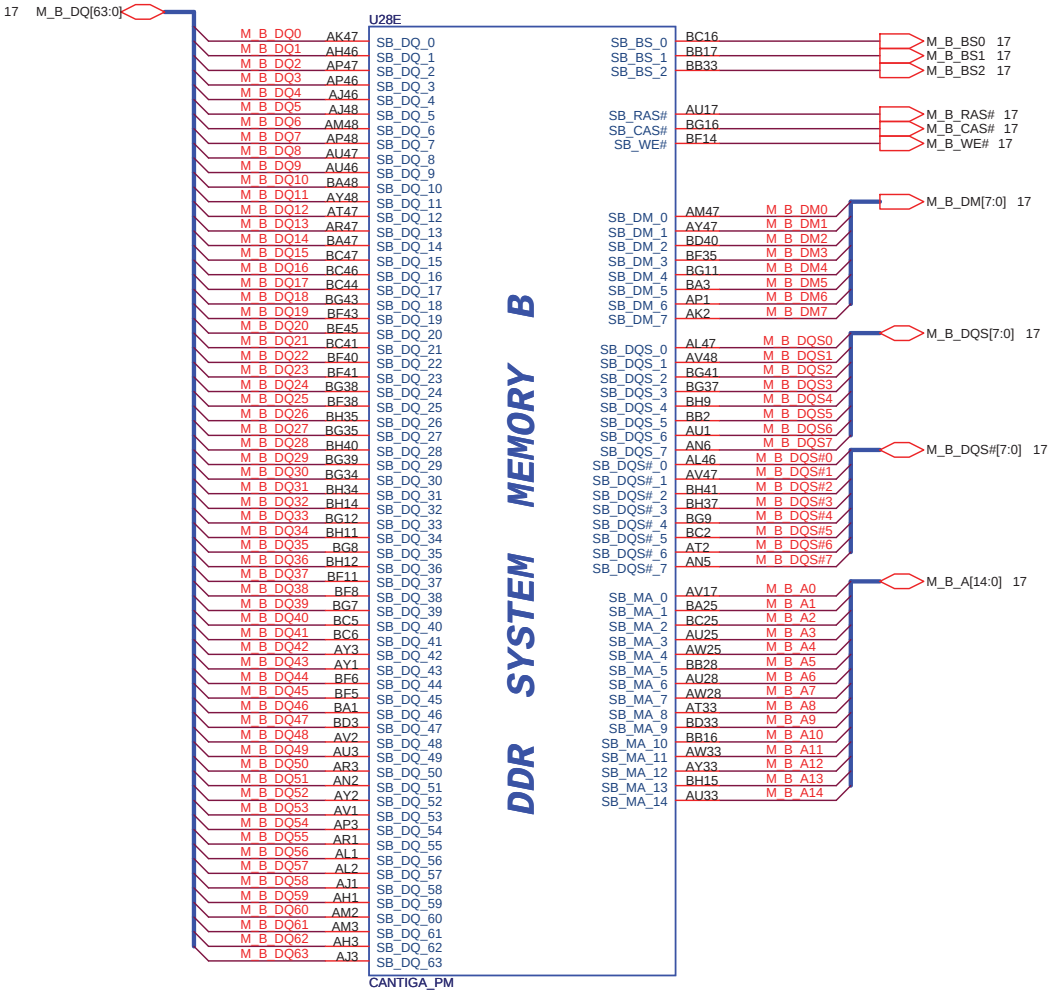
GMCH-CANTIGA(CLG)





Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	GMCH DDRIII		1A
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GMCH-CANTIGA(CLG)

IV@

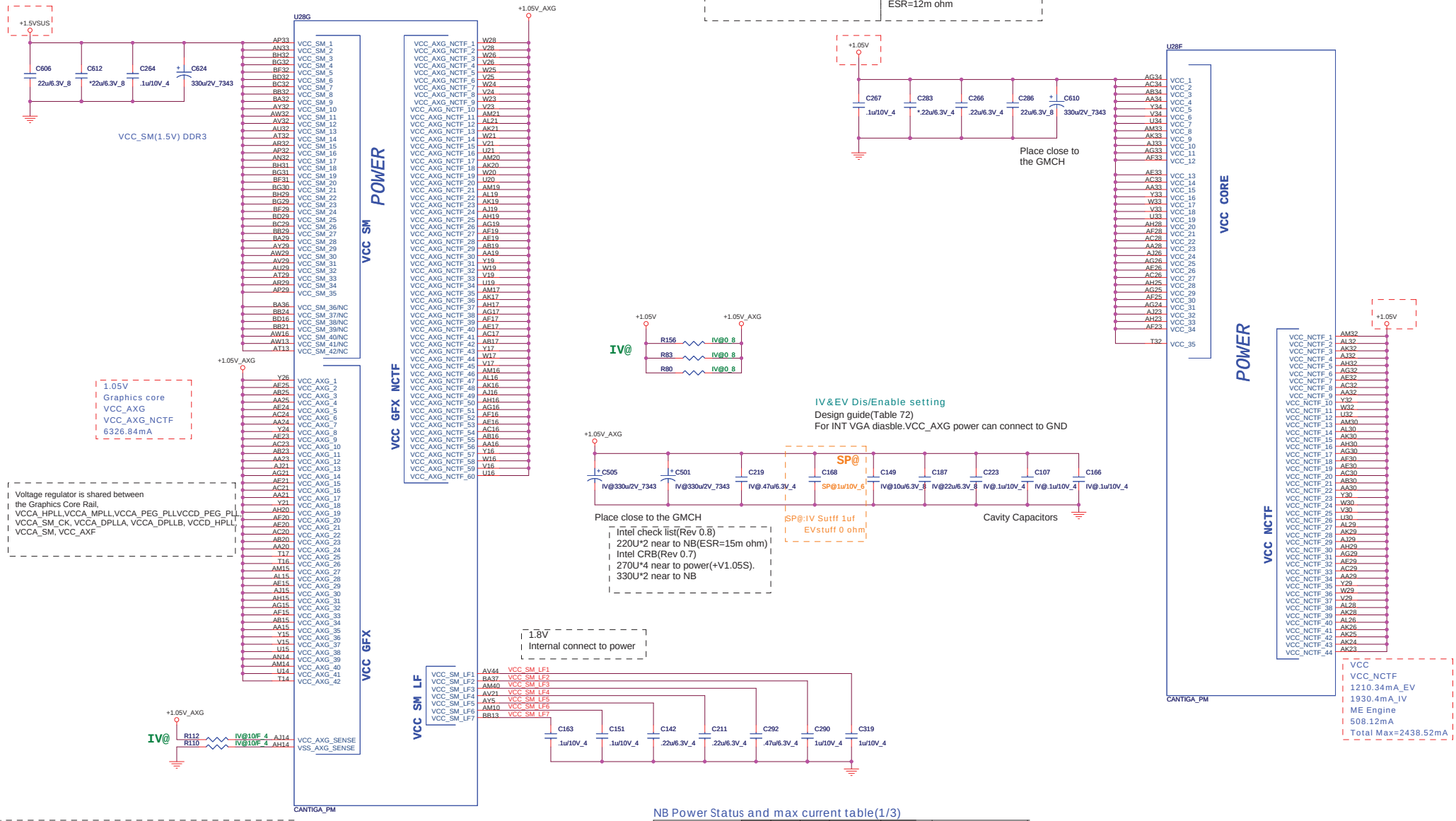
SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm
and VSS_AXG_SENSE PD with 10ohm for Intel suggest

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

Date: Monday, April 13, 2009 Sheet 9 of 42

GMCH-CANTIGA(CLG)

Power consumption reference to Intel Cantiga chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue STUFF 5.6 ohm

IV&EV Dis/Enable setting

+3V_CRT_TV_DAC R428 IV@0_6 +3V_VCCA_CRT_DAC C561 IV@.1u/10V_4 C560 SP@.01u/25V_4 C559 *IV@10u/6.3V_8

SP@:INT use 0.01U EXT use 0 ohm

R427 IV@0_6 +3V_A_DAC_BG C550 IV@.1u/10V_4 C551 SP@.01u/25V_4 C554 IV@10u/6.3V_8

3.3V 73mA

3.3V 5mA

USE same GND plane

SP@:INT use 0.1U EXT use 0 ohm

1210 10UH, 10% 0.45A DCR_max = 0.39

+1.05V L18 IV@10uH_8_155mA C577 IV@220u/2.5V_3528 C320 SP@.1u/10V_4 ESR=15 m

1.05V 64.8mA for DPLL_A/B

1210 10UH, 10% 0.45A DCR_max = 0.39

+1.05V L20 IV@10uH_8_155mA C573 IV@220u/2.5V_3528 C329 SP@.1u/10V_4 ESR=15 m

1.05V 24mA

VCCA_DPLLA/B always keep to +1.05V (If no use IV dynamic core power)

+1.05V R383 *short0603 C512 4.7u/6.3V_6 C517 .1u/10V_4

1.05V 139.2mA

1210 0.1uH, 20%, 1A, DCR_max=0.078Ω

L37 BKP1608HS181T_6_1.5A

+1.05VM_MPLL_RC R389 0.5/F_6 C504 22u/6.3V_8 C516 .1u/10V_4

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A DCR_max=90 m

3.3V 79mA

+3V L39 IV@BKP1608HS181T_6_1.5A C549 IV@10u/6.3V_8 C543 IV@.1u/10V_4 C542 SP@.01u/25V_4

IV&EV Dis/Enable setting

SP@:INT use 0.01U EXT use 0 ohm

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V 50mA

SP@:INT use 0.1U EXT use 0 ohm

+1.5V R438 IV@0_6 C571 SP@.1u/10V_4

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V 35mA

+1.5V R135 *short0603 C216 .1u/10V_4 C215 .01u/25V_4

1.5V
48.363mA for CRT
5mA for TV

FB 180@100 MHz, 25% 1.5A DCR_max=90 m

1.5V 0.5mA

L11 BKP1608HS181T_6_1.5A C226 10u/6.3V_8 C235 .1u/10V_4 C234 .01u/25V_4

CRB no 10U
Check list need min 10U~100U for VCCA_QDAC

MODIFY

FB 220 @100 MHz, 25%, 2A

1.05V 50mA

+1.05V L22 BKP1608HS181T_6_1.5A C344 .1u/10V_4 C346 .1u/10V_4

+1.05VM_PEGPLL_RC R208 1/F_4 C348 10u/6.3V_6

ESR=60m ohm

+1.8V R185 IV@0_6 +1.8V_DLVDS

1.8V 60.31mA

IV&EV Dis/Enable setting

SP@:INT use 1 U EXT use 0 ohm

C289 SP@1u/10V_4

U28H

CRT: VCCA_CRT_DAC_1 (B27), VCCA_CRT_DAC_2 (A26), VCCA_DAC_BG (A25), VSSA_DAC_BG (B25)

PLL: VCCA_DPLLA (F47) +1.05VM_DPLLA; VCCA_DPLLB (L48) +1.05VM_DPLLB; VCCA_HPLL (AD1) +1.05VM_HPLL; VCCA_MPLL (AE1) +1.05VM_MPLL

LVDS: VCCA_LVDS (J48) +1.8V_TXLVDS; VSSA_LVDS (J47)

PEG: VCCA_PEG_BG (AD48) +VCCA_PEG_BG; VCCA_PEG_PLL (AA48) +1.05VM_PEGPLL

SM: VCCA_SM_1 (AP20), VCCA_SM_2 (AN20), VCCA_SM_3 (AR17), VCCA_SM_4 (AP17), VCCA_SM_5 (AN17), VCCA_SM_6 (AT16), VCCA_SM_7 (AR16), VCCA_SM_8 (AP16), VCCA_SM_9

CK: VCCA_SM_CK_1 (AP28), VCCA_SM_CK_2 (AN28), VCCA_SM_CK_3 (AP25), VCCA_SM_CK_4 (AN25), VCCA_SM_CK_5 (AN24), VCCA_SM_CK_NCTF_1 (AM28), VCCA_SM_CK_NCTF_2 (AM26), VCCA_SM_CK_NCTF_3 (AM25), VCCA_SM_CK_NCTF_4 (AL25), VCCA_SM_CK_NCTF_5 (AM24), VCCA_SM_CK_NCTF_6 (AL24), VCCA_SM_CK_NCTF_7 (AM23), VCCA_SM_CK_NCTF_8 (AL23)

TV: VCCA_TV_DAC_1 (B24) +3V_CRT_TV_DAC; VCCA_TV_DAC_2 (A24)

HDA: VCC_HDA (A32) +VCCD_HDA

D TV/CRT: VCCD_TVDAC (M25) +1.5V_TVDAC; VCCD_QDAC (L28) +1.5V_QDAC; VCCD_HPLL (AF1) +1.05VM_MCH_PLL2; VCCD_PEG_PLL (AA47) +1.05VM_PEGPLL

LVDS: VCCD_LVDS_1 (M38), VCCD_LVDS_2 (L37)

CANTIGA_PM

VCCD_QDAC share to TV and CRT

+1.05V R390 *short0603 C515 .1u/10V_4

1.05V 157.2mA

POWER

VTT: VTT_1 (U13), VTT_2 (T13), VTT_3 (U12), VTT_4 (T12), VTT_5 (U11), VTT_6 (T11), VTT_7 (U10), VTT_8 (T10), VTT_9 (U9), VTT_10 (T9), VTT_11 (U8), VTT_12 (T8), VTT_13 (U7), VTT_14 (T7), VTT_15 (U6), VTT_16 (T6), VTT_17 (U5), VTT_18 (T5), VTT_19 (V3), VTT_20 (U3), VTT_21 (V2), VTT_22 (U2), VTT_23 (T2), VTT_24 (V1), VTT_25 (U1)

+1.05V_VCCP_GMCH C171 .47u/6.3V_4 C119 2.2u/6.3V_6 C118 4.7u/6.3V_6 C131 4.7u/6.3V_6 R91 *short0805 +1.05V C527 330u/2V_7343

1.05V FSB-1067 852mA

ESR= 12m ohm

+1.05VM_AXF C538 1u/10V_4 C536 *10u_8 R418 *short0805 +1.05V

1.05V 321.35mA

ESR = 60 m

1.8V DDR2-800 124mA

0805 1UH , Rdc = 0.14 - 0.26. Max rated current = 220 mA

+1.5VSUS_VCC_SM_CK C544 .1u/10V_4 R307 *short0805 +1.5VSUS

1/F_4 R421 +1.8VSUS_SMCK_RC C537 10u/6.3V_6

AXF: VCC_AXF_1 (B22), VCC_AXF_2 (B21), VCC_AXF_3 (A21)

SM CK: VCC_SM_CK_1 (BF21), VCC_SM_CK_2 (BH20), VCC_SM_CK_3 (BG20), VCC_SM_CK_4 (BF20)

VCC_TX_LVDS (K47)

HV: VCC_HV_1 (C35), VCC_HV_2 (B35), VCC_HV_3 (A35)

PEG: VCC_PEG_1 (V48), VCC_PEG_2 (U48), VCC_PEG_3 (V47), VCC_PEG_4 (U47), VCC_PEG_5 (U46)

DMI: VCC_DMI_1 (AH48), VCC_DMI_2 (AF48), VCC_DMI_3 (AH47), VCC_DMI_4 (AG47)

VTTLF: VTTLF1 (A8) VTTLF1, VTTLF2 (L1) VTTLF2, VTTLF3 (AB2) VTTLF3

C518 .47u/6.3V_4 C519 .47u/6.3V_4 C526 .47u/6.3V_4

1.05V
Internal connect to power

IV&EV Dis/Enable setting

+1.8V_TXLVDS R209 IV@0_8 +1.8V C345 SP@1000p/50V_4 C347 *IV@22u/6.3V_8

SP@:INT use 1000pf EXT use 0 ohm

1.8V 118.8mA

3.3V 105.3mA

+3V C291 .1u/10V_4 R193 10_4 +1.05V_SD D13 CH751 +1.05V

+1.05V_VCC_PEG C328 4.7u/6.3V_6 C607 22u/6.3V_8 C613 220u/2.5V_3528 R466 *short0805 +1.05V

1.05V 1782mA

1.05V 456mA

C589 .1u/10V_4

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	GMCH POWER	1A

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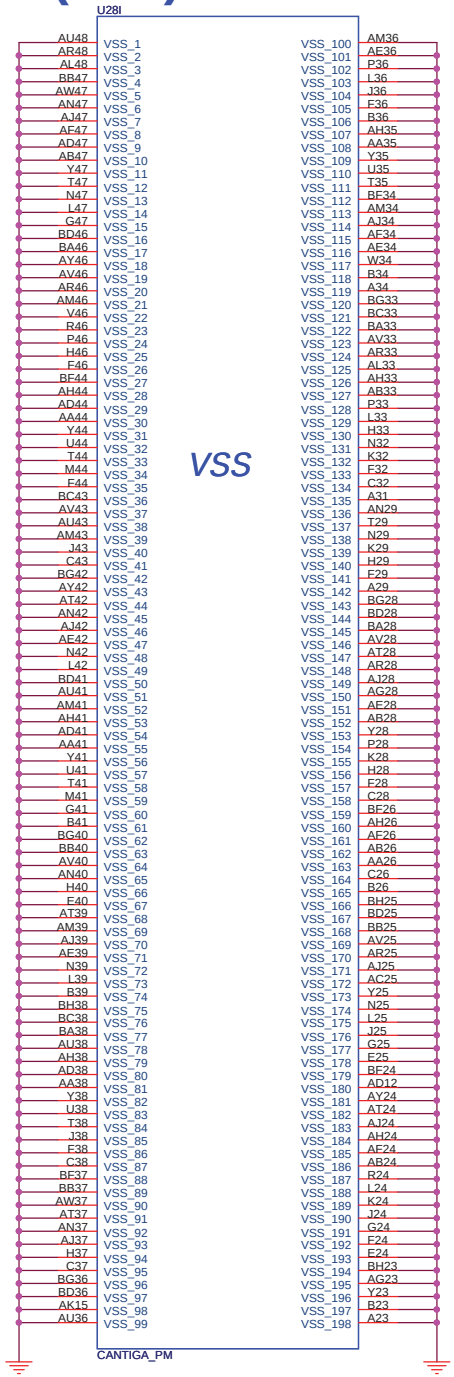
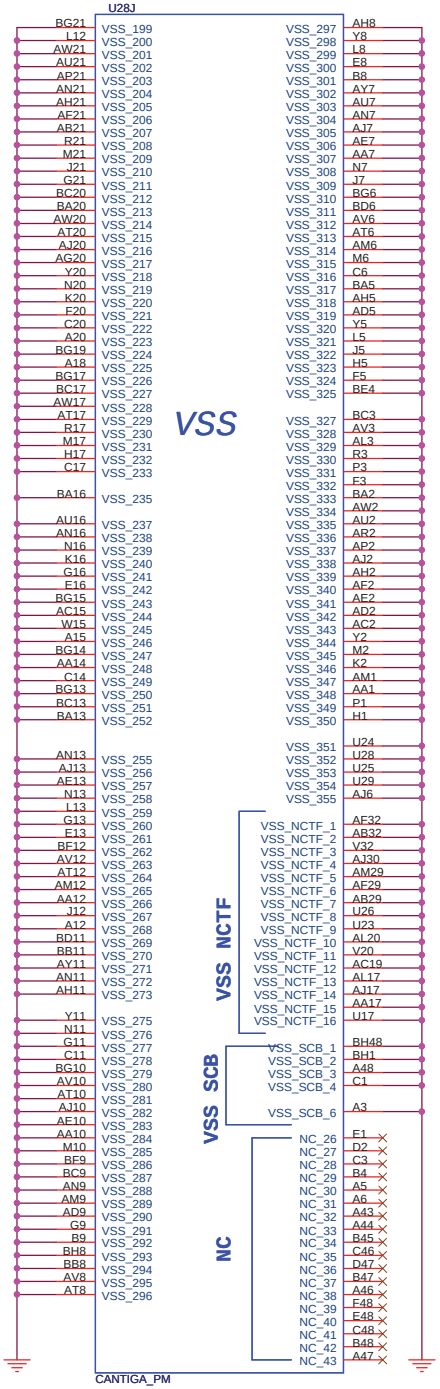
GMCH-CANTIGA(CLG)





Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	GMCH VSS	1A

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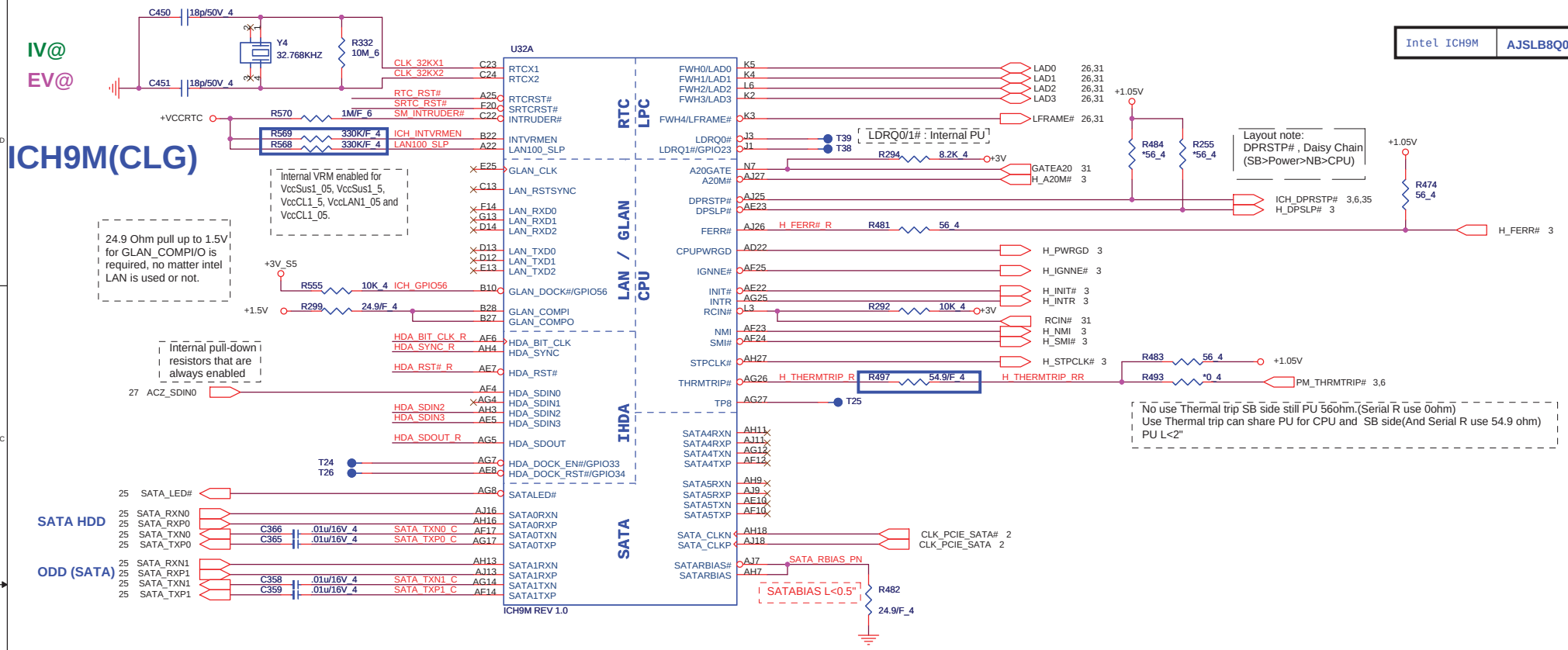
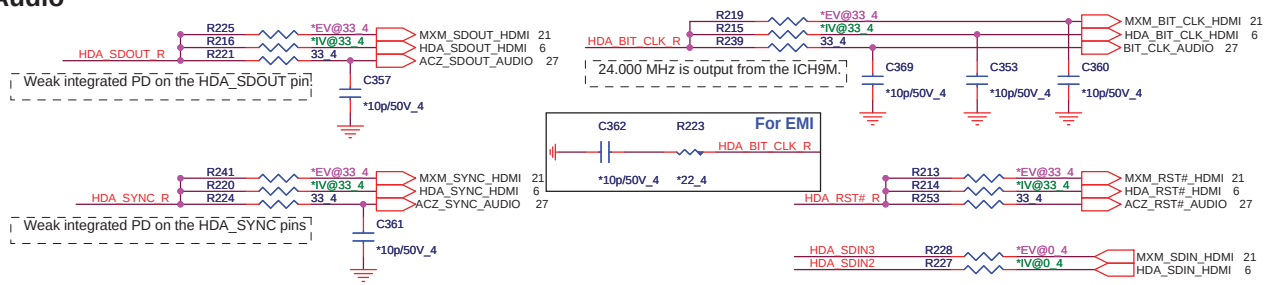
IV@

EV@

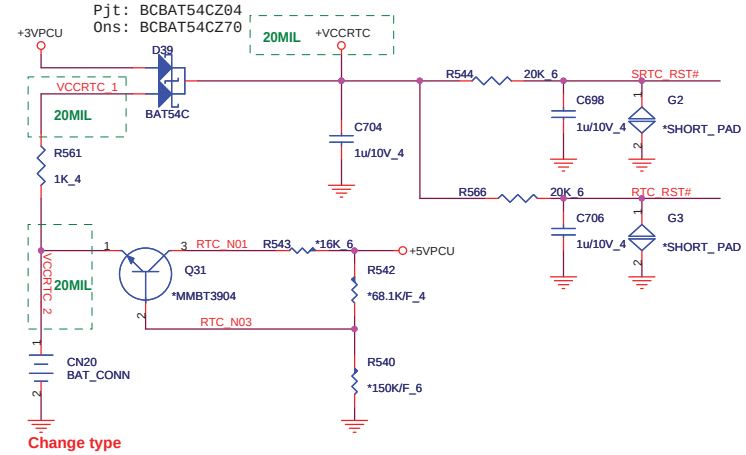
ICH9M(CLG)



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	14 ICH_TP3 — ICH_TP3 R545 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R240 *1K_4 +3V

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	ICH9M HOST	1A

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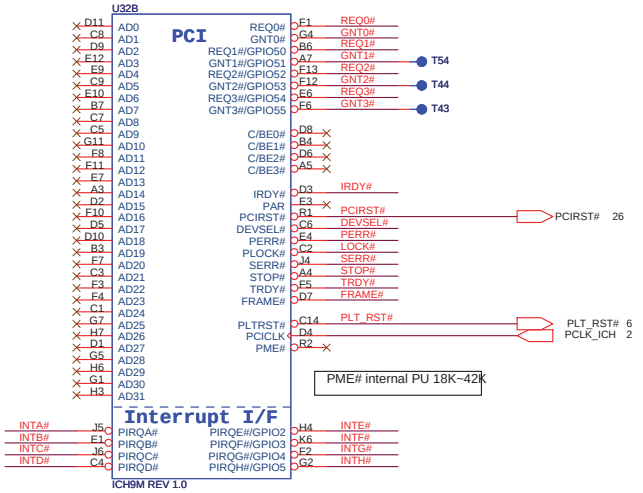
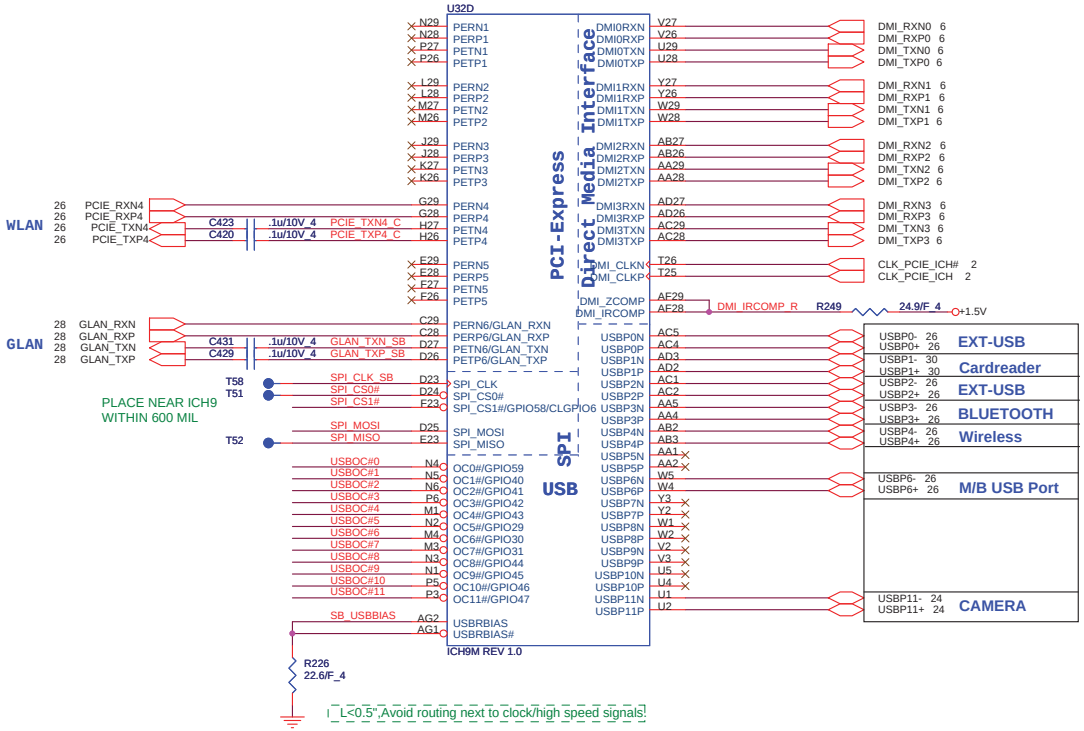
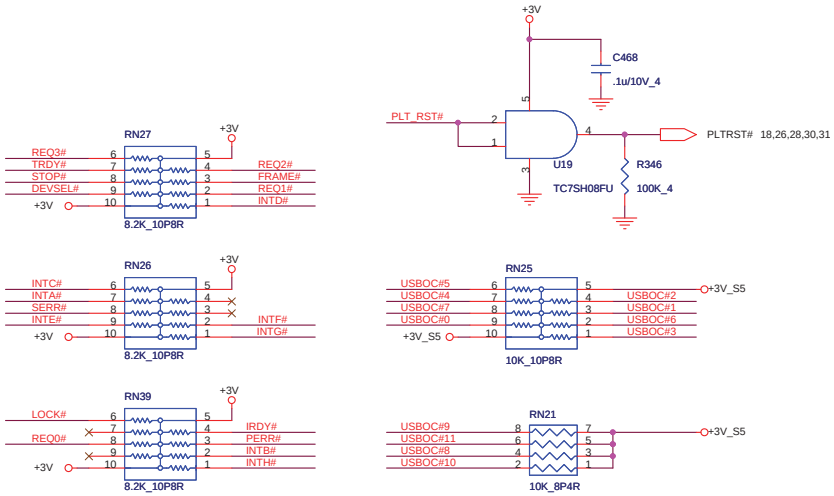
ICH9M(CLG)







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R309 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R277 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R293 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R274 *1K_4

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A

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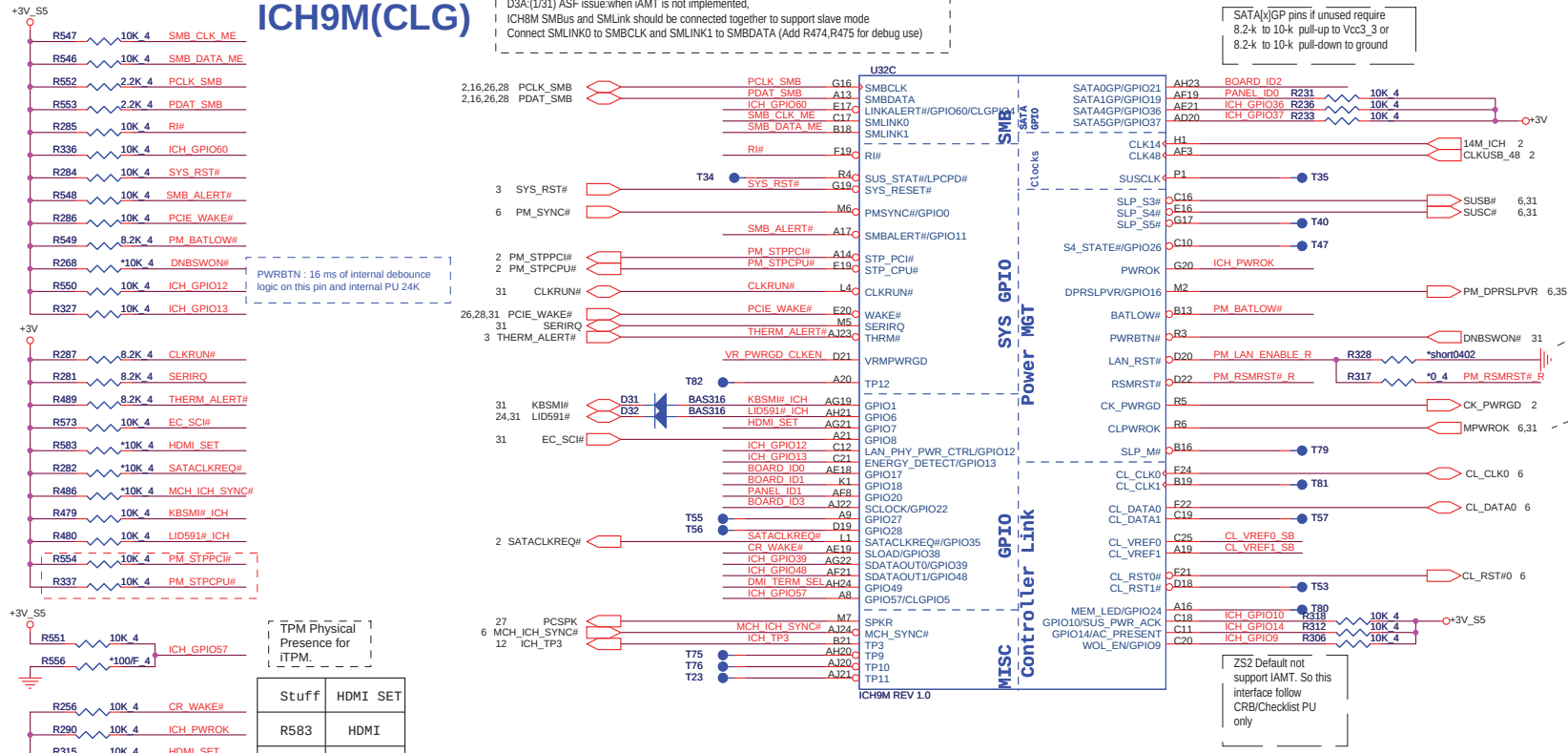
ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground

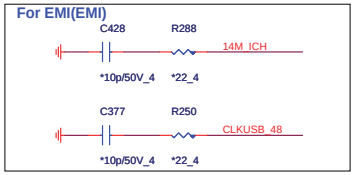


Stuff	HDMI SET
R583	HDMI
R315	No HDMI

<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

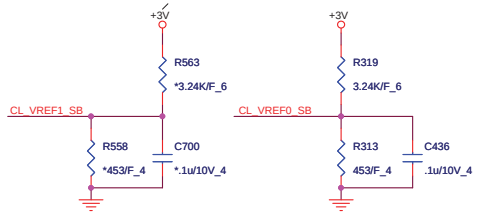
For EMI(EMI)

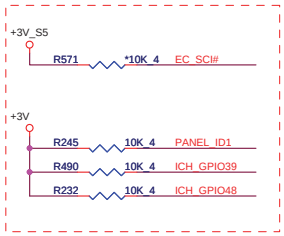


CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

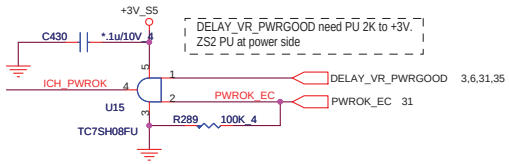
<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.



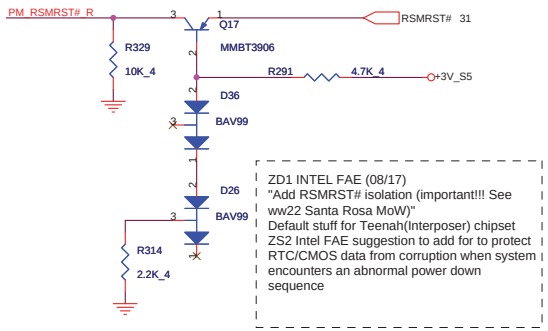


Follow CHECK LIST V1.5

ICH PWROK



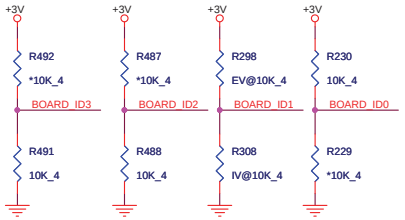
Resume RST



ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

ID0=0 -->ZK6 ,ID0=1 -->ZR6
ID1=0 -->UMA ,ID1=1 -->Discrete

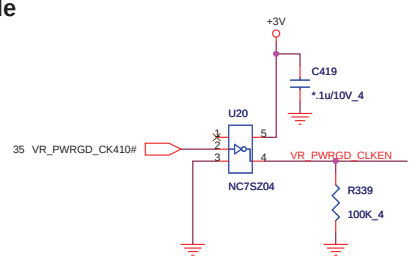


Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZR6

Size	Document Number	Rev
	ICH9M GPIO	1A

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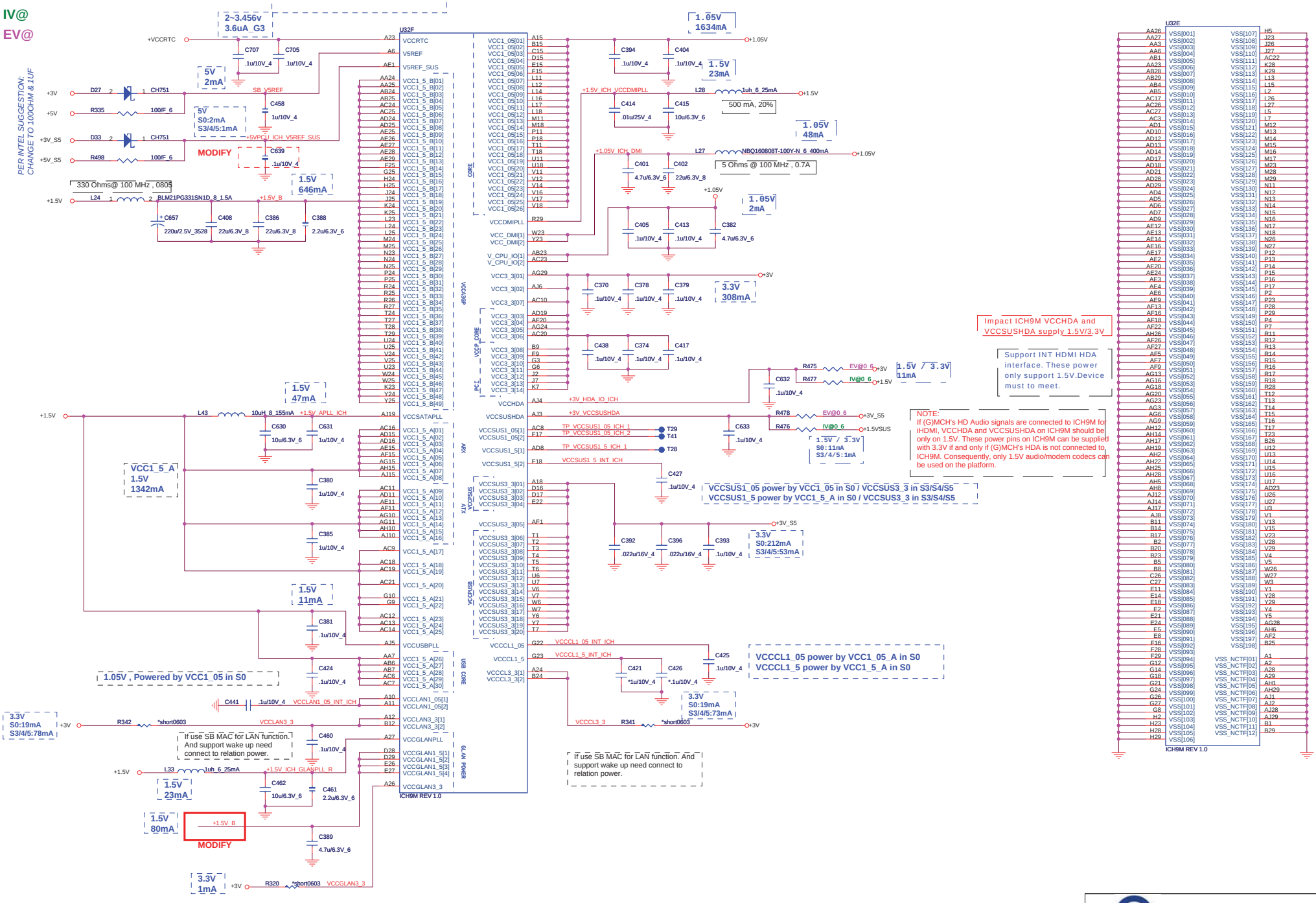
ICH9M(CLG)

IV@
EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF



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PROJECT : ZR6		
Size	Document Number: ICH9 POWER	Rev 1A
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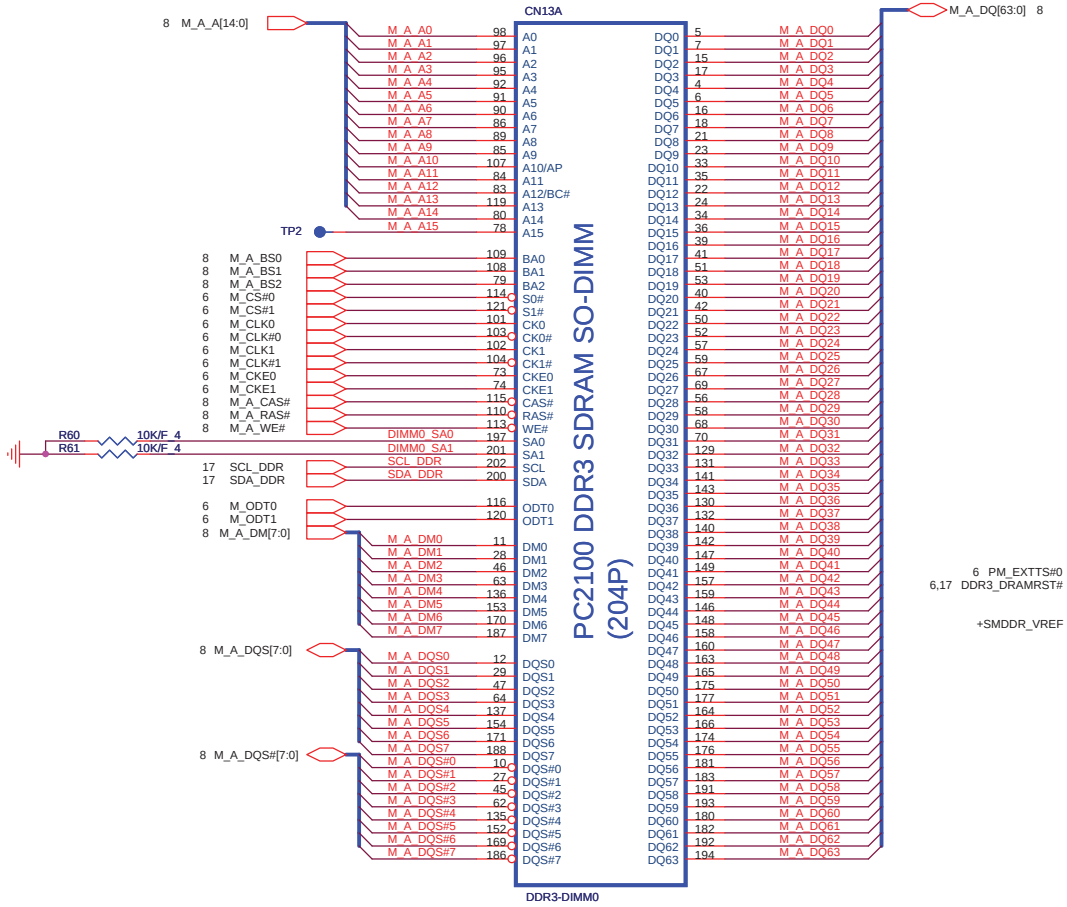
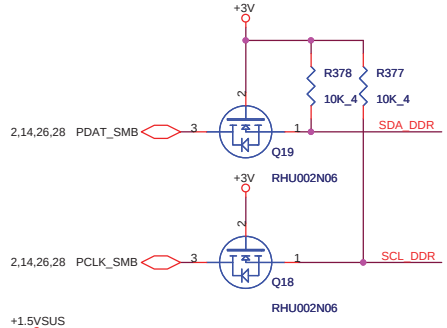
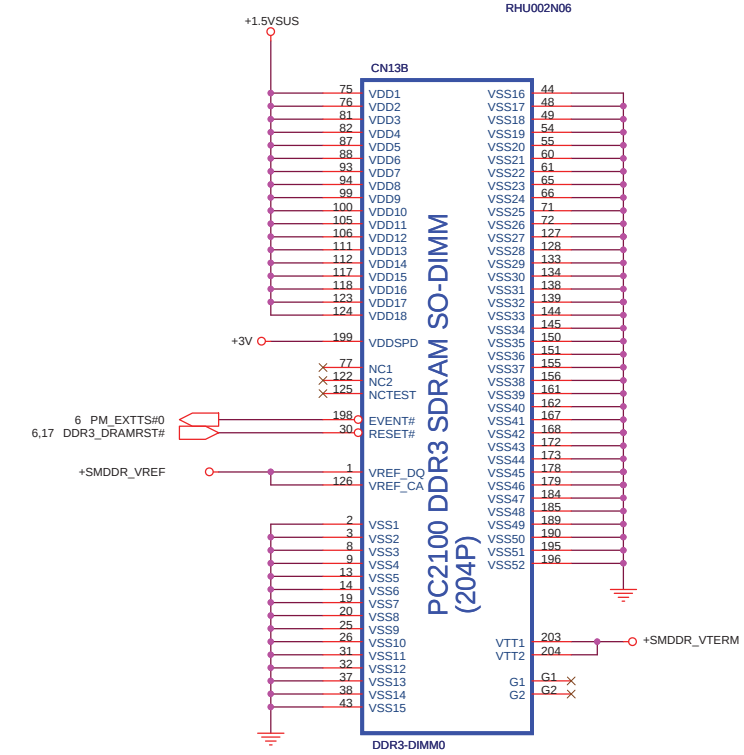
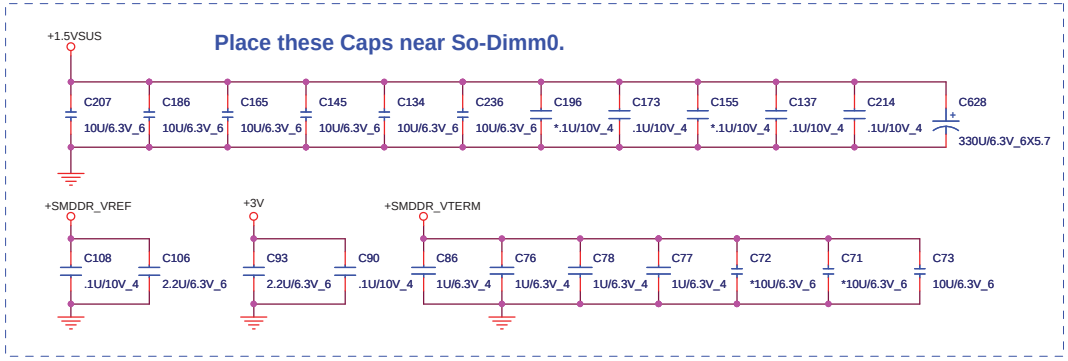
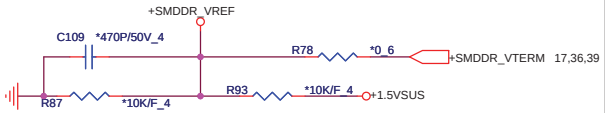
DDR3 (DDR)











Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number: DDR3 DIMM-0(H=5.2)	Rev 1A
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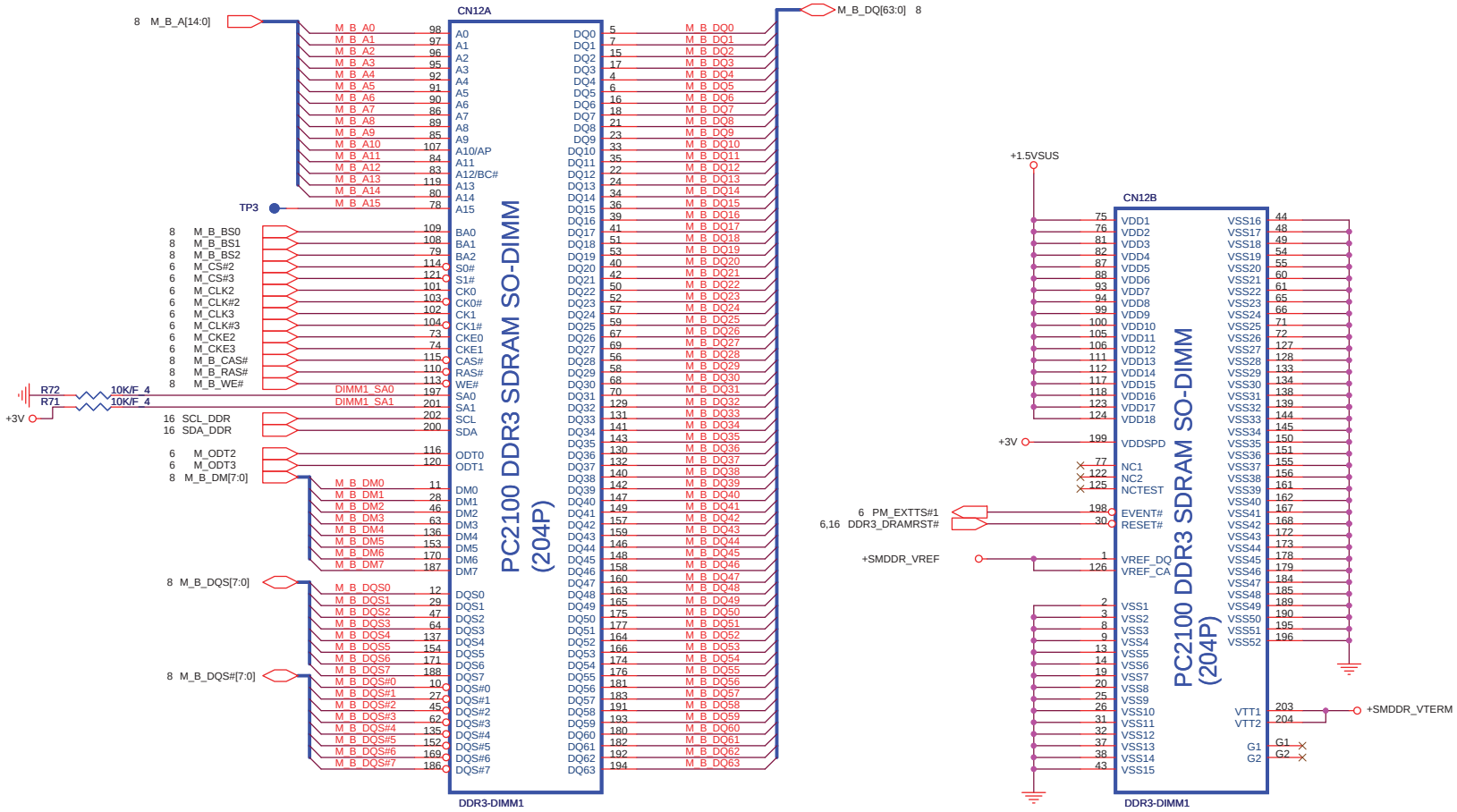
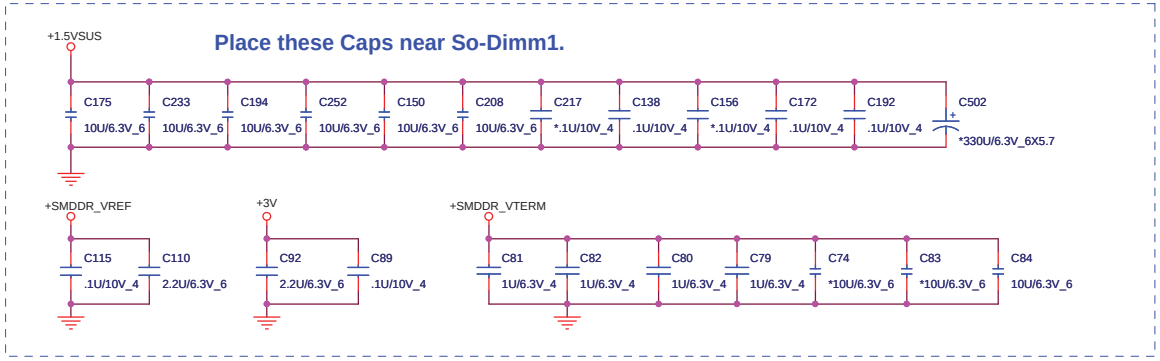
DDR3 (DDR)





Quanta Computer Inc.		
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Size	Document Number: DDR3 DIMM-1(H=9.2)	Rev 1A
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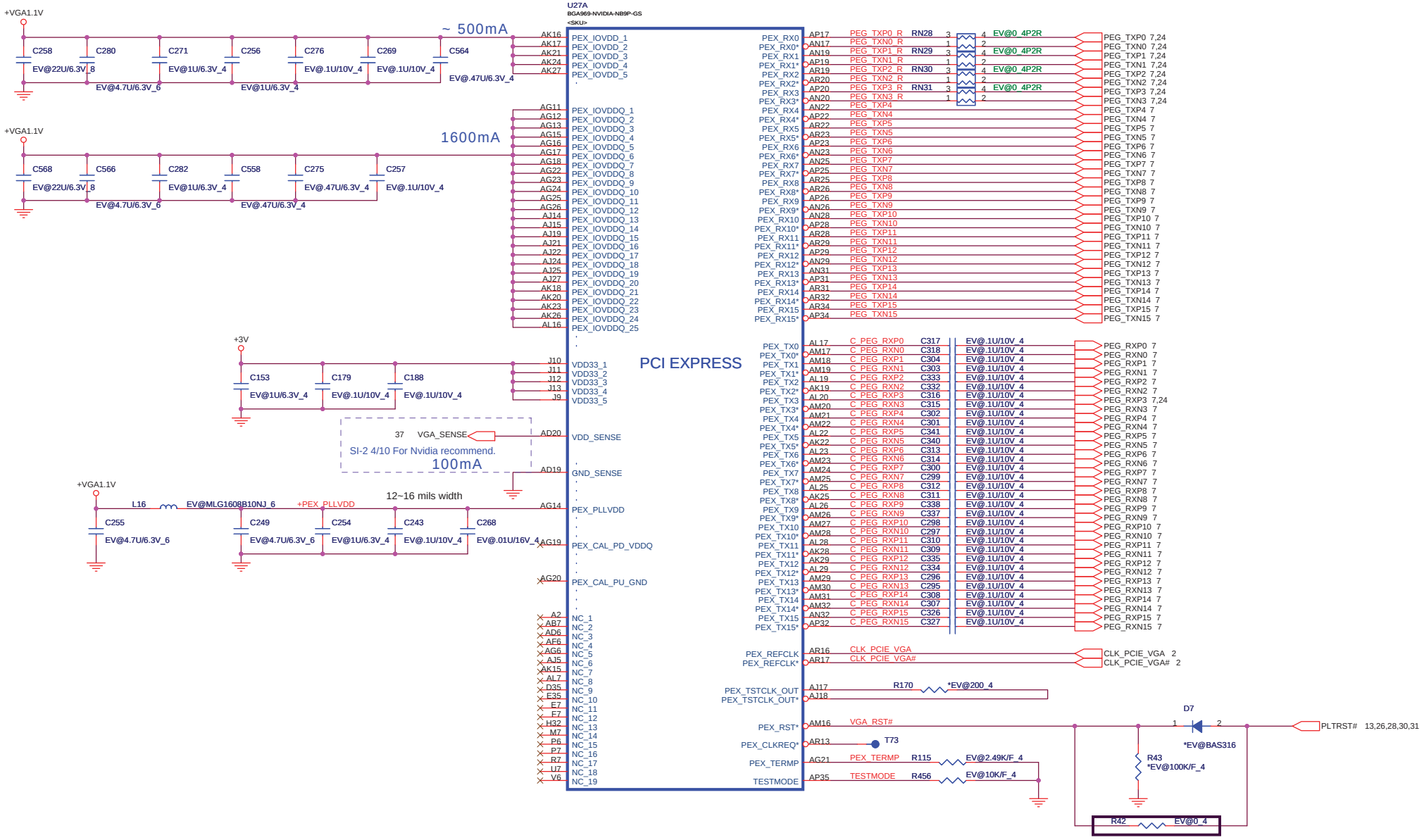
NV10M (VGA)

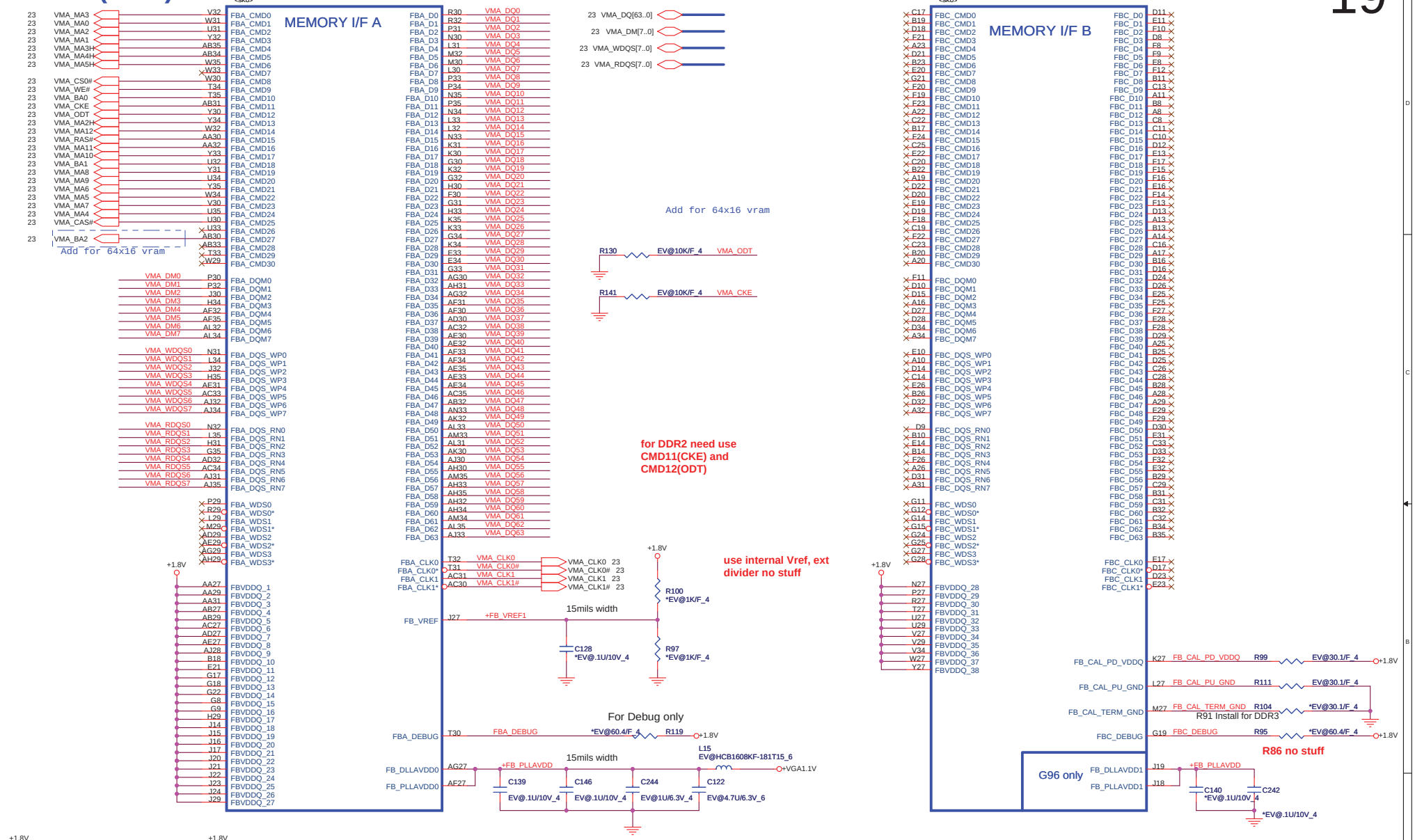


Size	Document Number		Rev
	NV10X (PCIE I/F) 1/5		1A
Date: Monday, April 13, 2009		Sheet 18 of 42	

Quanta Computer Inc.

PROJECT : ZR6

NV10M (VGA)



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	NV10X (MEMORY I/F) 2/5	1A

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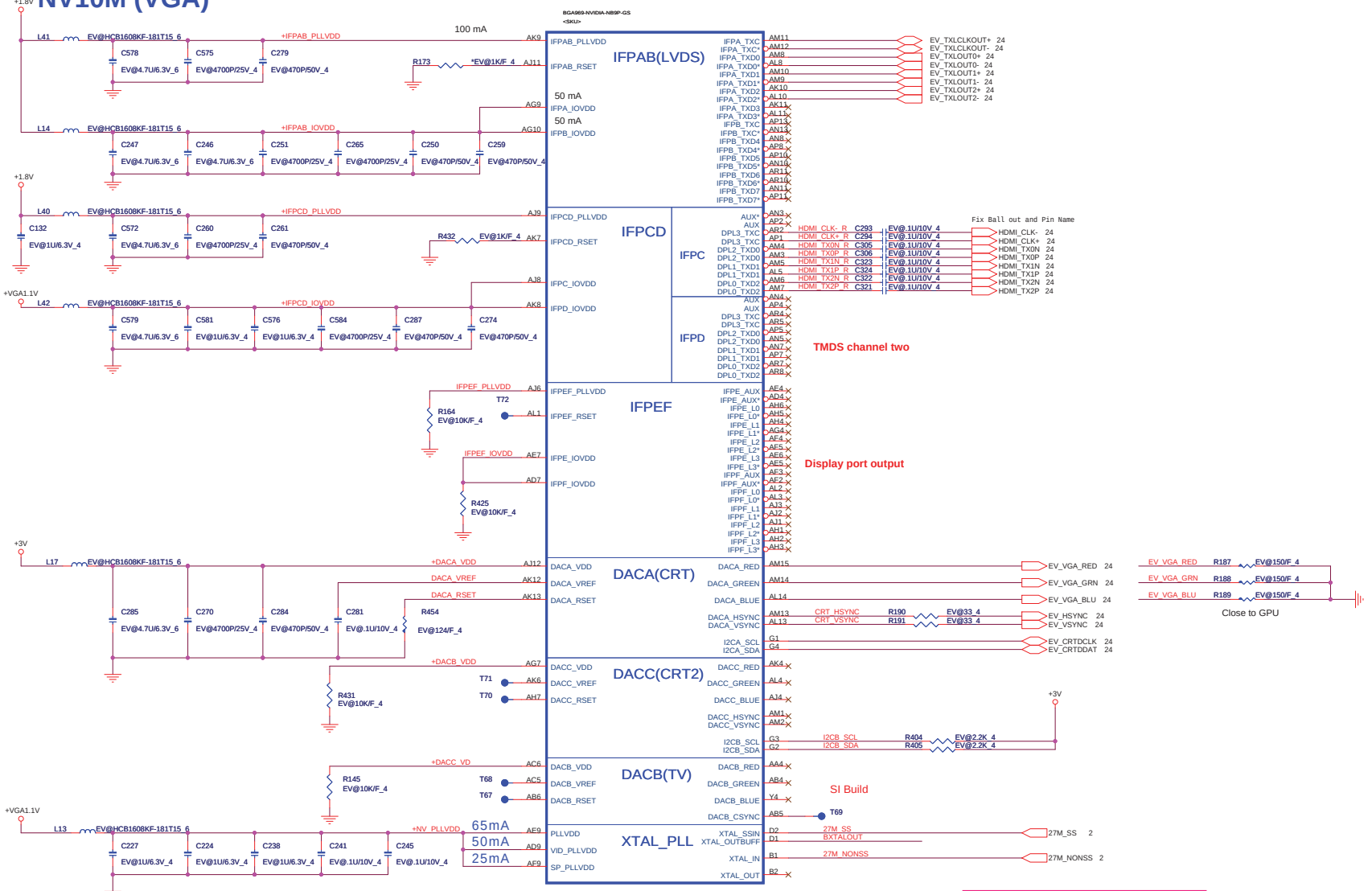
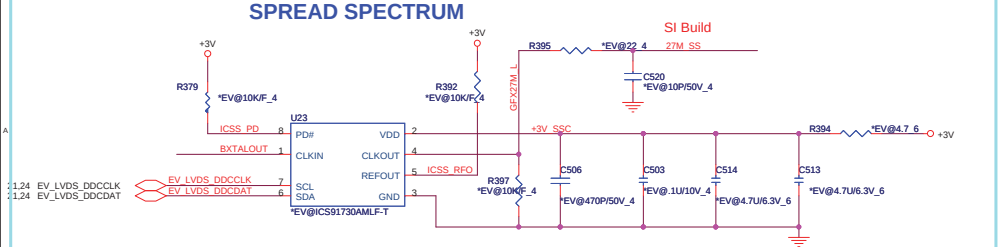
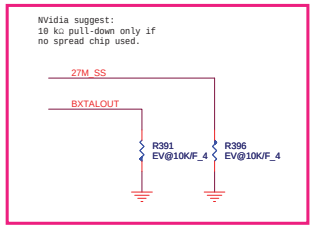
NV10M (VGA)



SPREAD SPECTRUM



I2C ADDRESS: 0xD4H



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Size	Document Number	Rev
	NV10X (DISPLAY) 3/5	1A

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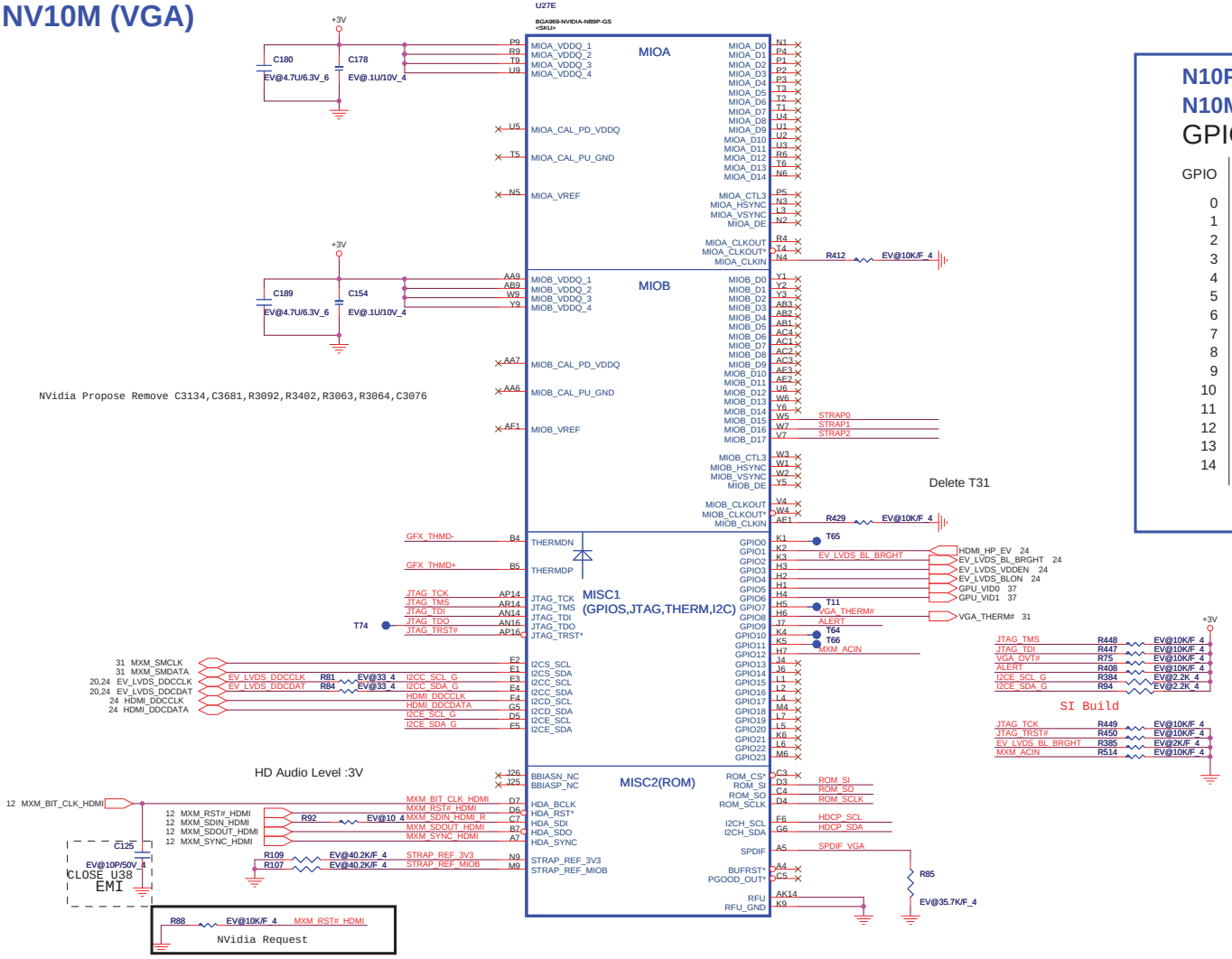
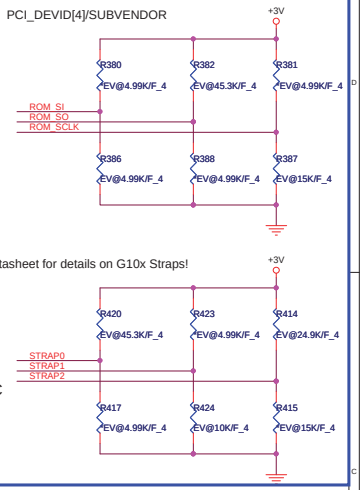
NV10M (VGA)



N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



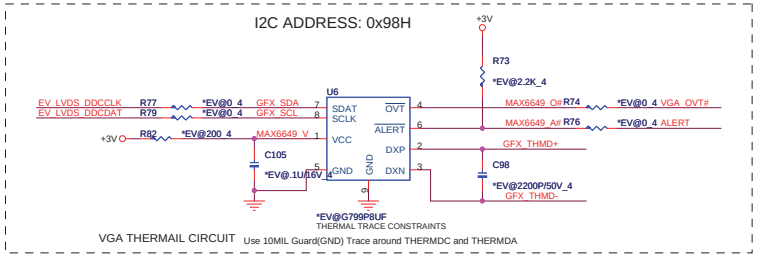
PCI_DEVID: STRAP2

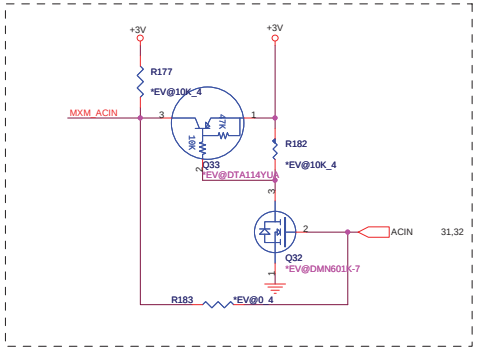
NB9M-GE	0x06E	8	1000	
NB9M-GS	0x06E	9	1001	
NB9P-GE2	0x064	8	1000	
NB9P-GS	0x064	9	1001	
N10P-GE1	0x065	2	0010	
N10M-GE1	0x06E	C	1100	default

Logical Strap Bit Mapping

R414	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

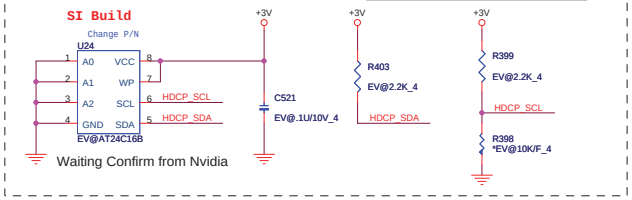
R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E





HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM **Hi: I2C ROM**



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Size	Document Number	Rev
	NV10X (GPIO & STRRAPS) 4/5	1A

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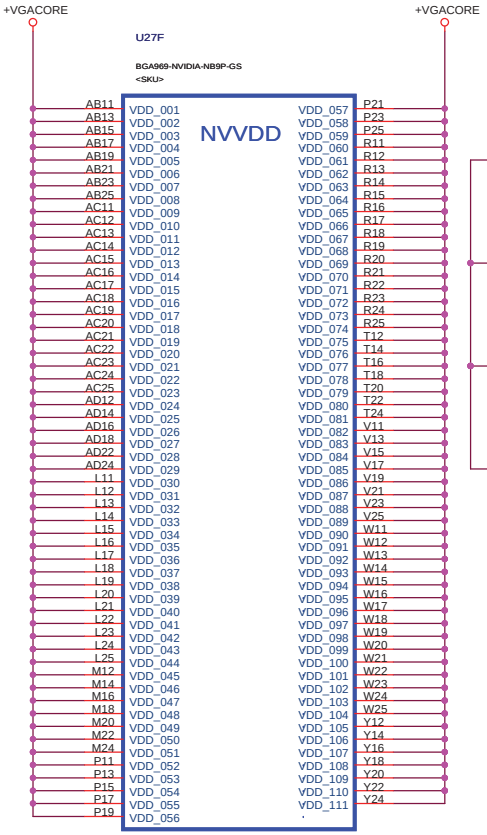
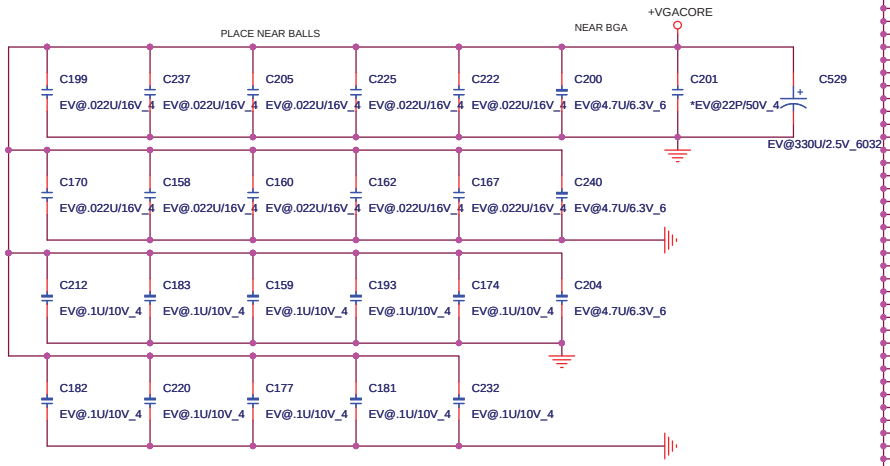
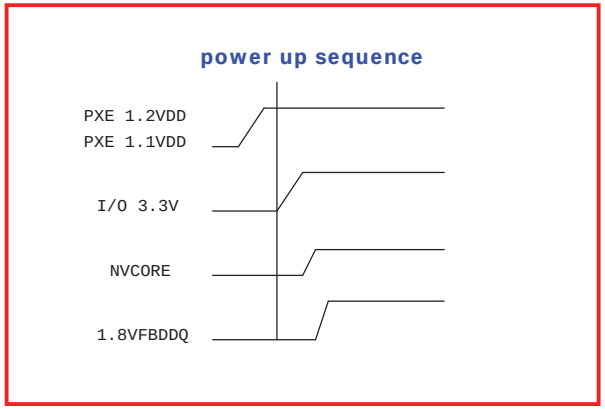
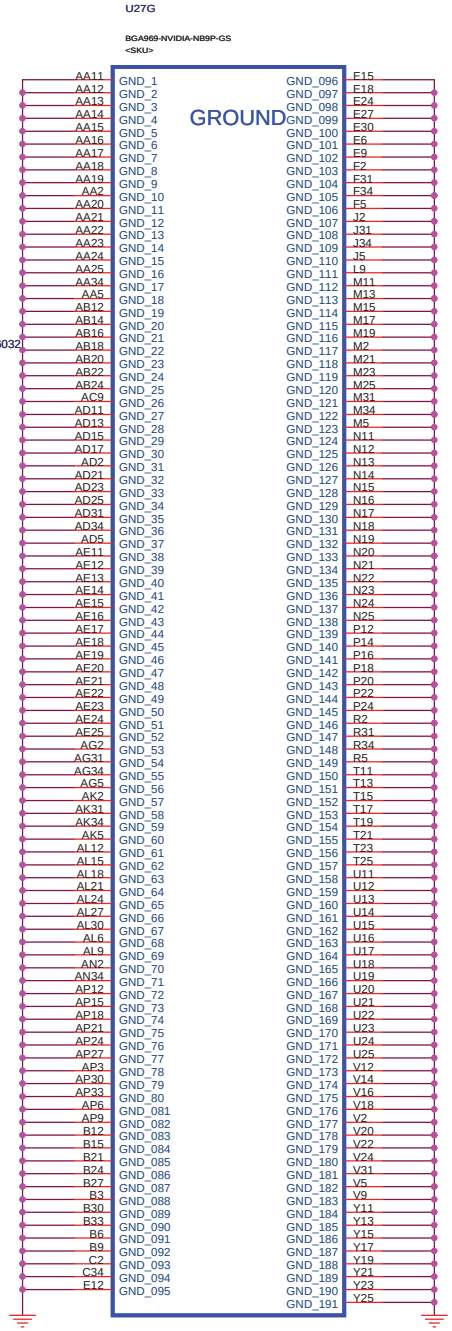
NVVDD Decoupling





Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10





Quanta Computer Inc.		
PROJECT : ZR6		
Size	Document Number	Rev
	NV10X (POWER & GND) 5/5	1A
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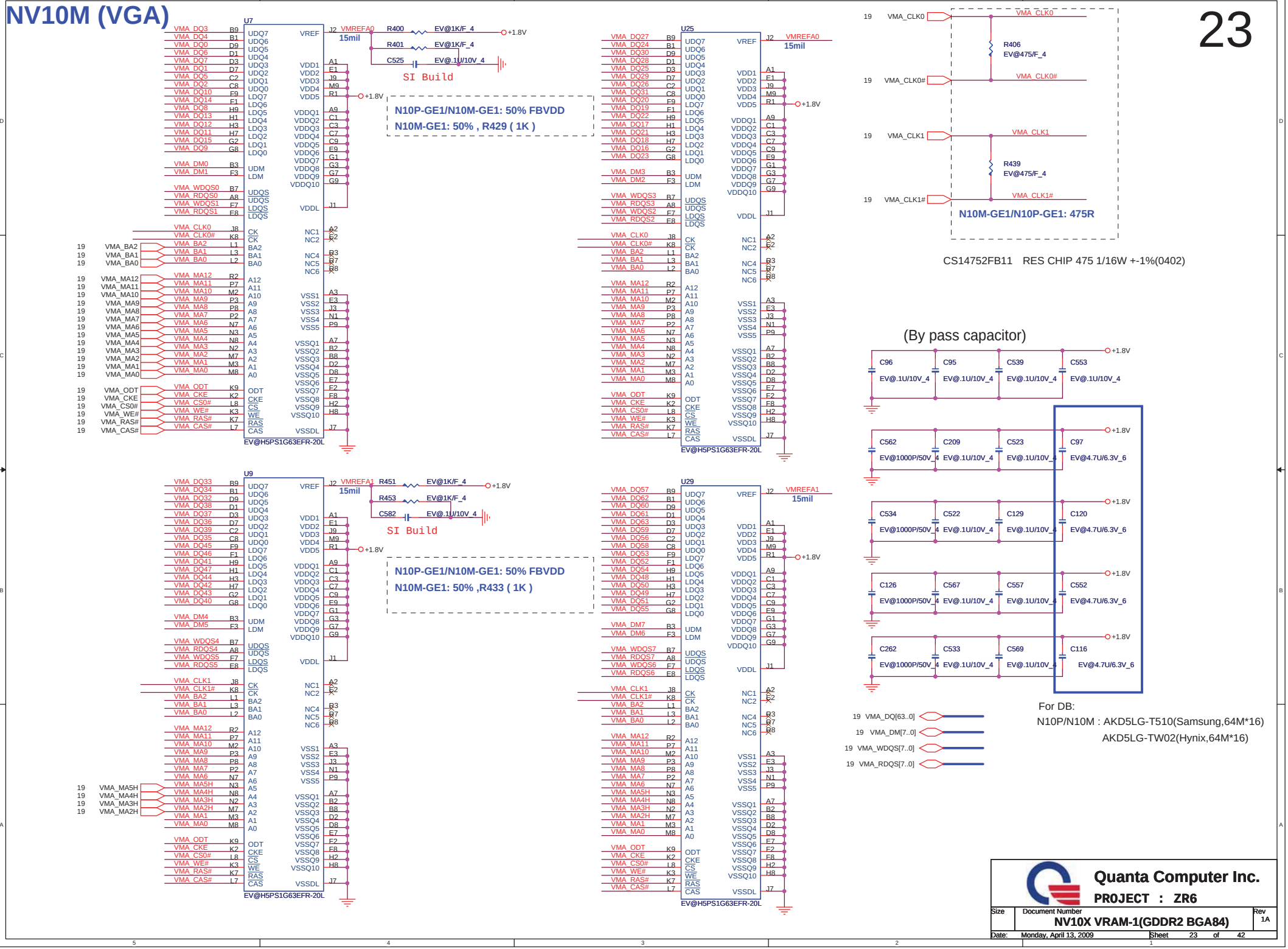
NV10M (VGA)


U7
U25
U9
U29
EV@H5PS1G63EFR-20L
VMREFA0
VMREFA1
15mil
R400 EV@1K/F_4
R401 EV@1K/F_4
C525 EV@.1U/10V_4
R451 EV@1K/F_4
R453 EV@1K/F_4
C582 EV@.1U/10V_4
+1.8V
SI Build
N10P-GE1/N10M-GE1: 50% FBVDD
N10M-GE1: 50% , R429 (1K)
N10P-GE1/N10M-GE1: 50% FBVDD
N10M-GE1: 50% ,R433 (1K)
R406 EV@475/F_4
R439 EV@475/F_4
N10M-GE1/N10P-GE1: 475R
CS14752FB11 RES CHIP 475 1/16W +-1%(0402)
(By pass capacitor)
C96 EV@.1U/10V_4
C95 EV@.1U/10V_4
C539 EV@.1U/10V_4
C553 EV@.1U/10V_4
C562 EV@1000P/50V_4
C209 EV@.1U/10V_4
C523 EV@.1U/10V_4
C97 EV@4.7U/6.3V_6
C534 EV@1000P/50V_4
C522 EV@.1U/10V_4
C129 EV@.1U/10V_4
C120 EV@4.7U/6.3V_6
C126 EV@1000P/50V_4
C567 EV@.1U/10V_4
C557 EV@.1U/10V_4
C552 EV@4.7U/6.3V_6
C262 EV@1000P/50V_4
C533 EV@.1U/10V_4
C569 EV@.1U/10V_4
C116 EV@4.7U/6.3V_6
19 VMA_DQ[63..0]
19 VMA_DM[7..0]
19 VMA_WDQS[7..0]
19 VMA_RDQS[7..0]
For DB:
N10P/N10M : AKD5LG-T510(Samsung,64M*16)
AKD5LG-TW02(Hynix,64M*16)
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Size
Document Number
NV10X VRAM-1(GDDR2 BGA84)
Rev
1A
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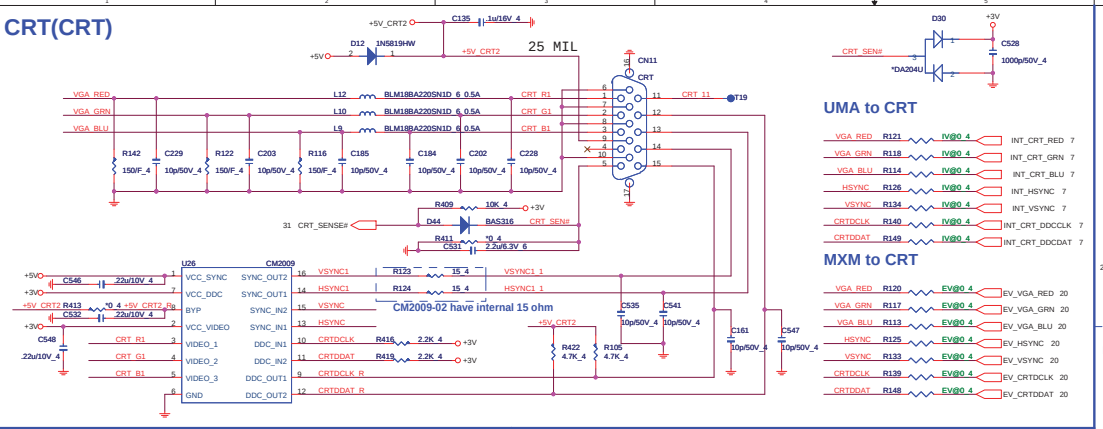
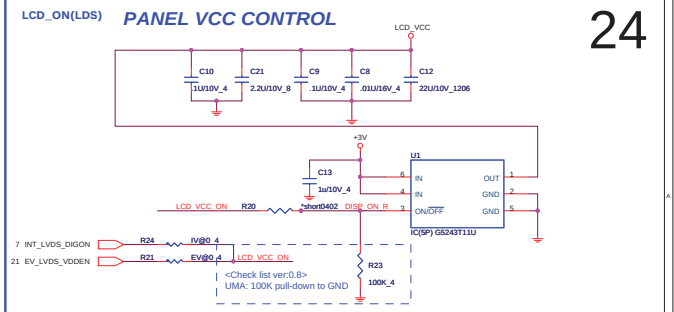
CRT(CRT)



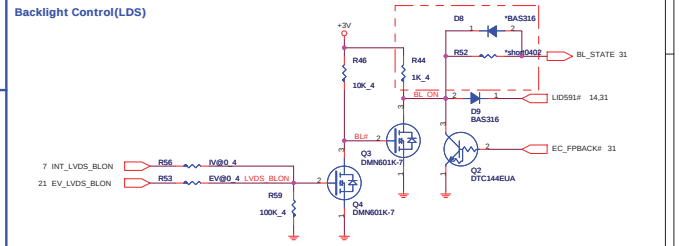
UMA to CRT

MXM to CRT

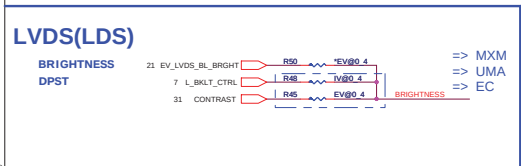
LCD_ON(LDS) PANEL VCC CONTROL



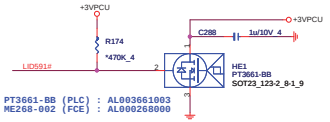
Backlight Control(LDS)



LVDS(LDS)



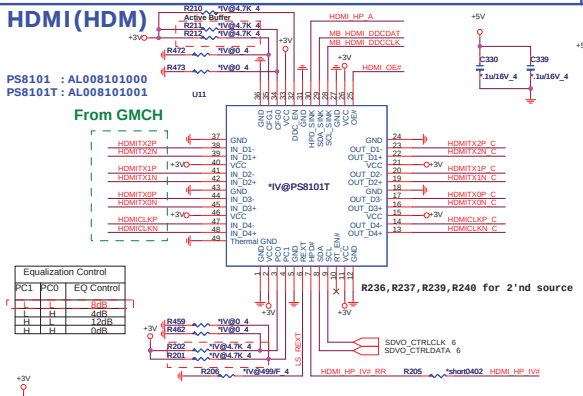
Lid Switch (HSR)

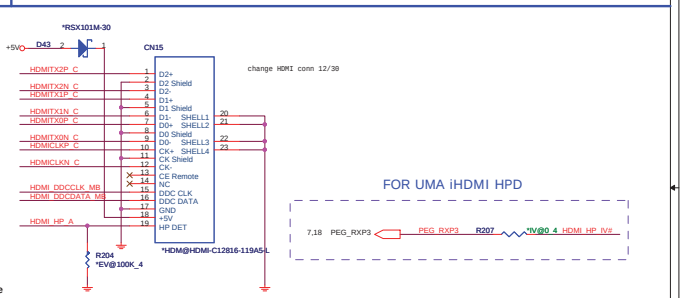


LCD EDID SMBus PU

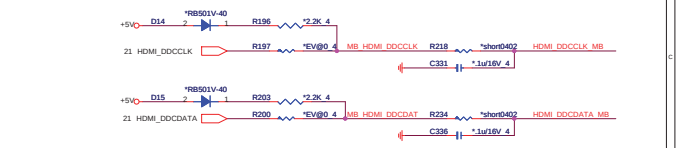
HDMI(HDM)

PS8101 : AL008101000
PS8101T : AL008101001

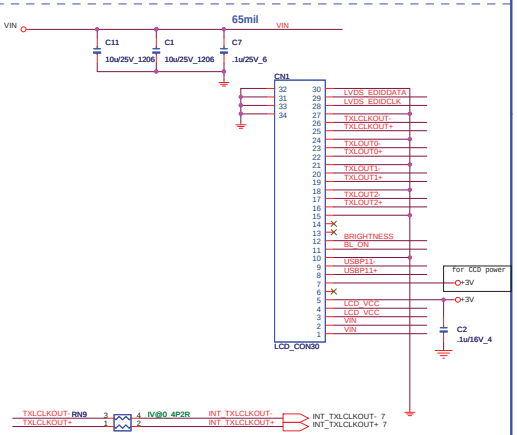




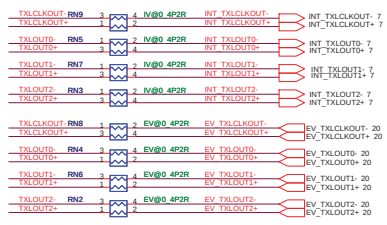
SDVO I2C Control



65mil

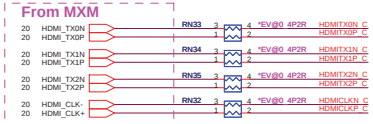


UMA to LVDS



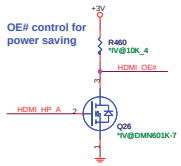
MXM to LVDS

From MXM

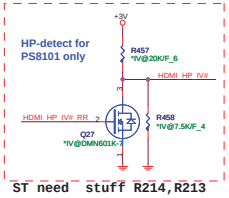


From GMCH (iHDMI)

OE# control for power saving

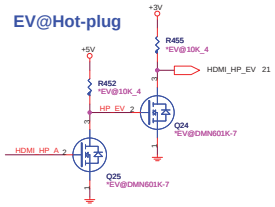


HP-detect for PS8101 only



ST need stuff R214,R213

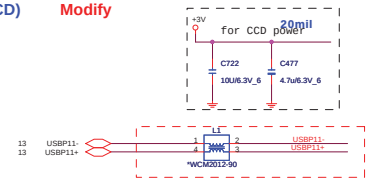
EV@Hot-plug



FOR NV HDMI

NV suggestion near HDMI connector

Camera(CCD) Modify



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Size	Document Number	Rev
	LVDS/CRT/CCD/HDMI/MIC	1A

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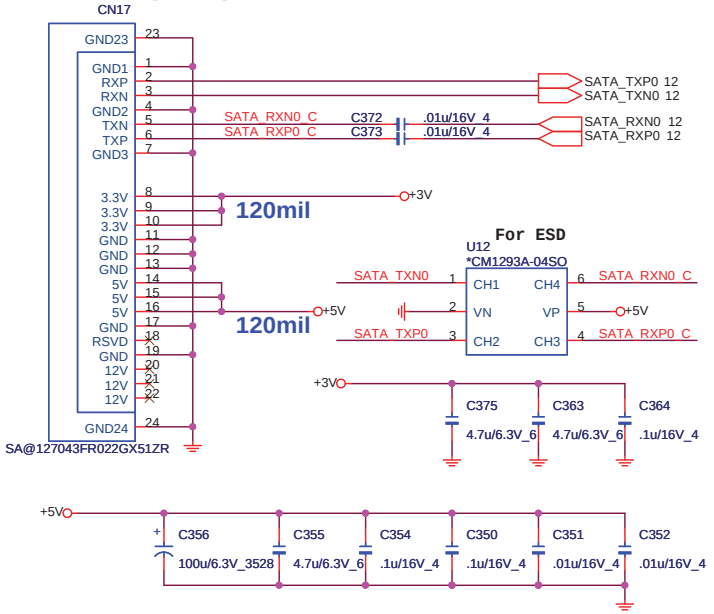
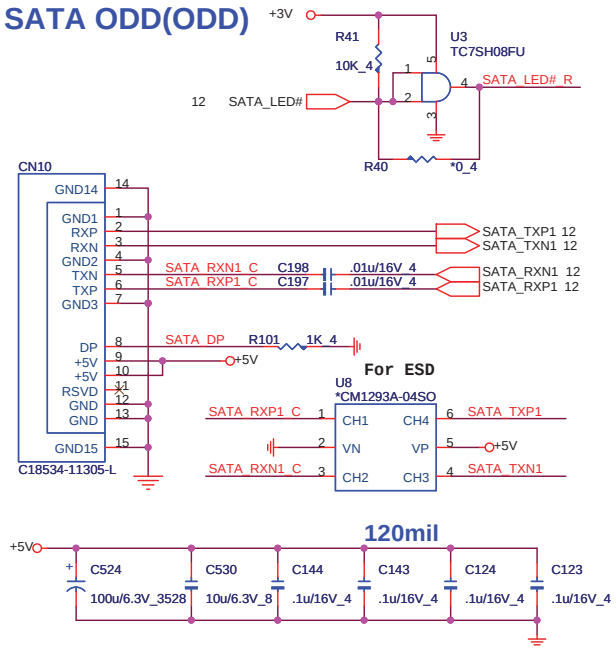
SATA HDD(HDD)

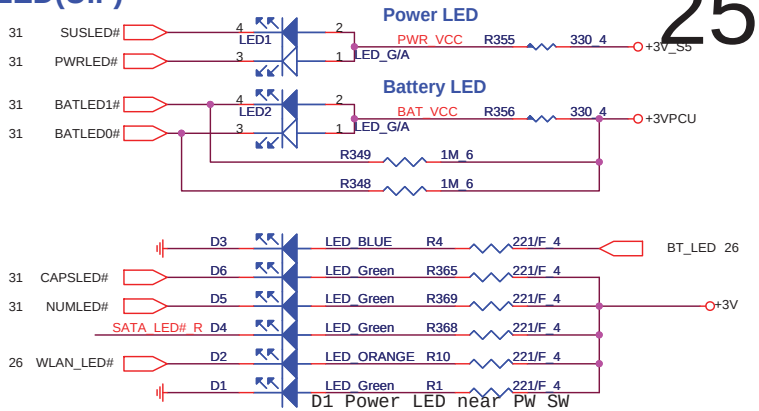


SATA ODD(ODD)

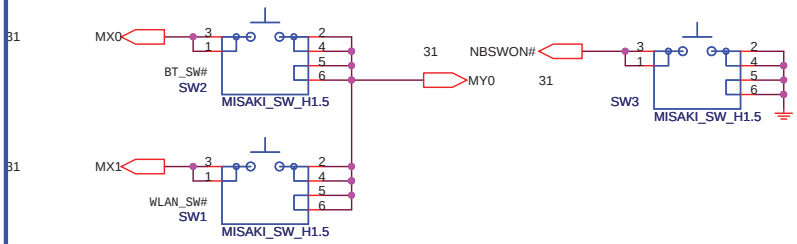


LED(UIF)

Power/Suspend: Green/Amber

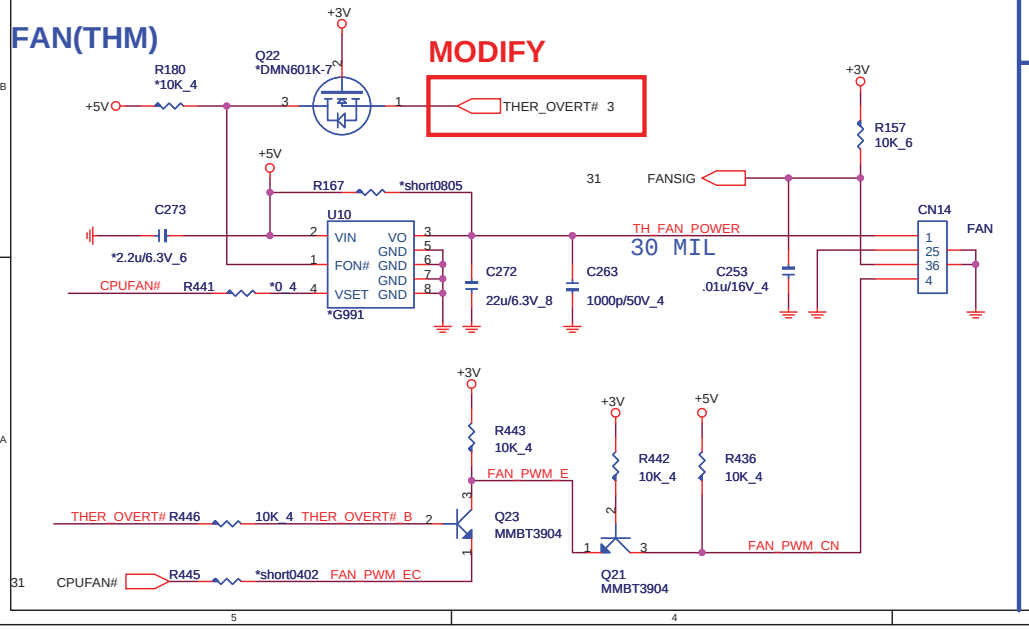


Power Button (UIF)



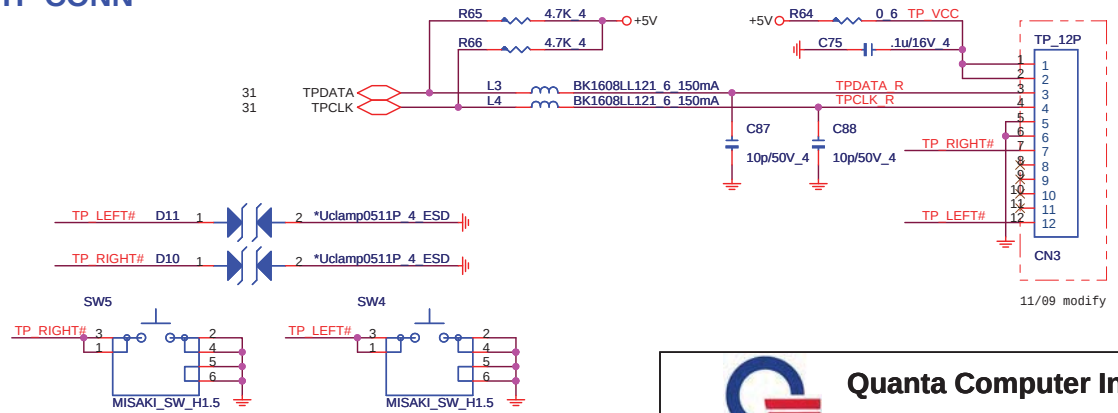
FAN(THM)

MODIFY



TP CONN

25mil



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Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A

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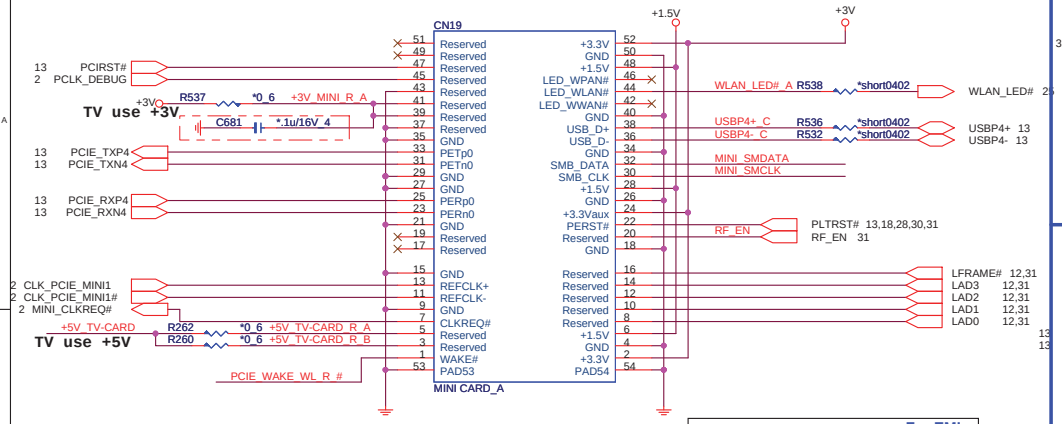
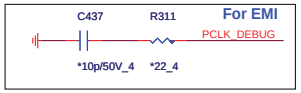
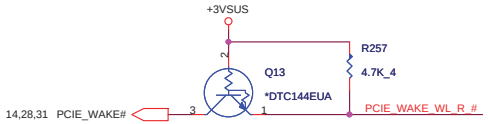
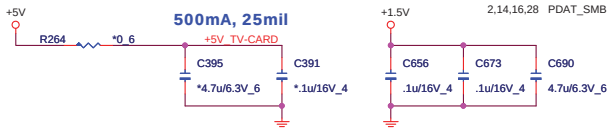
MINI-CARD(MPC)

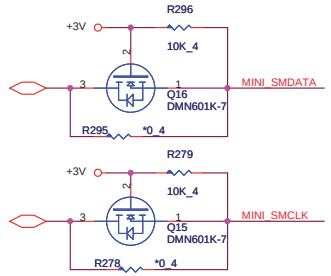


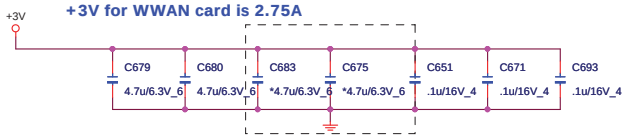
For EMI



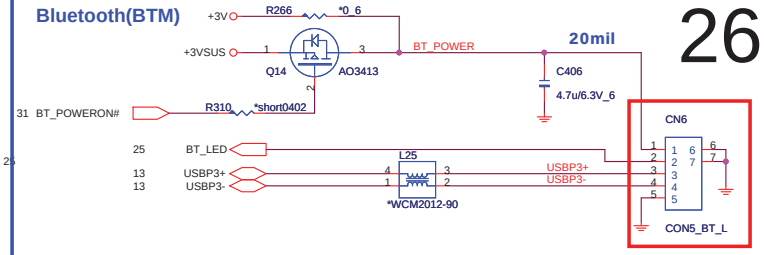






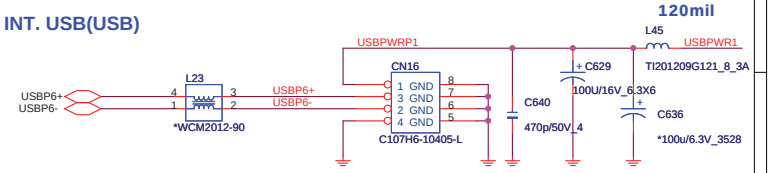


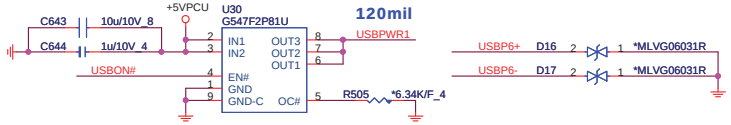
Bluetooth(BTM)



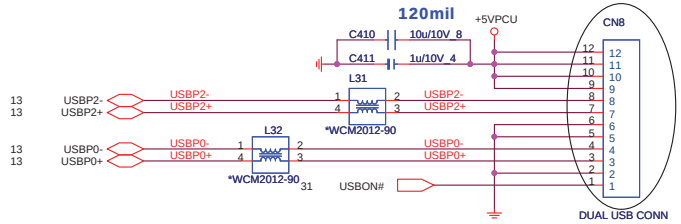
MODIFY Follow Z07

INT. USB(USB)



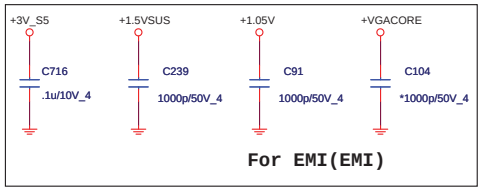


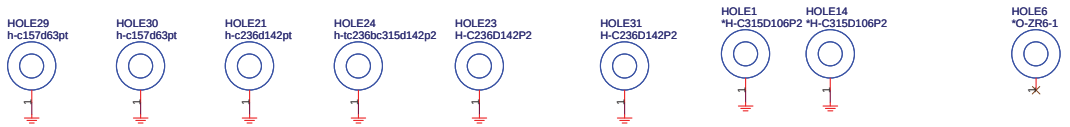
EXT. USB(USB)

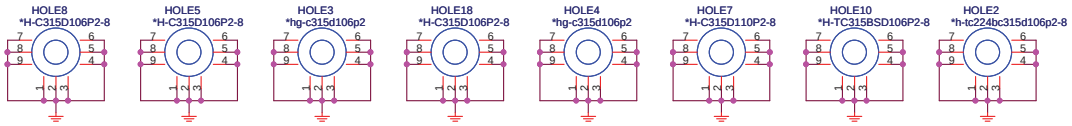


Modfiy C

(OTH)







Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A

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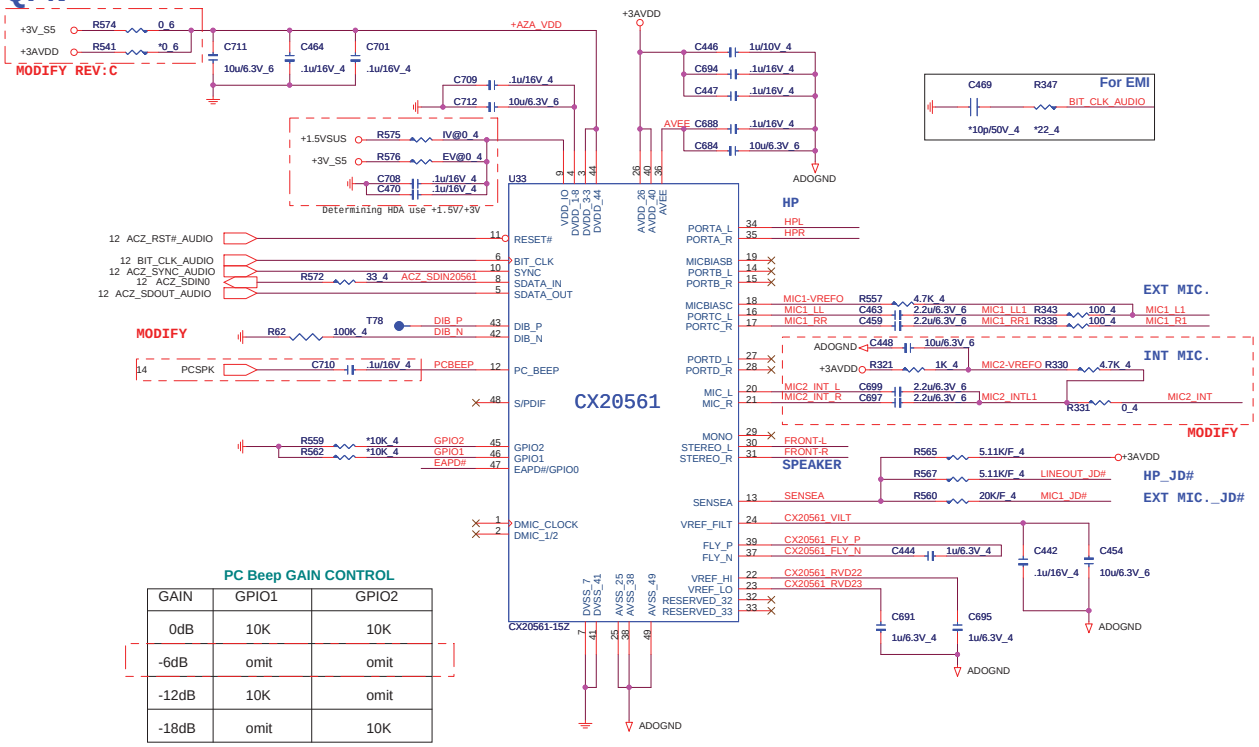
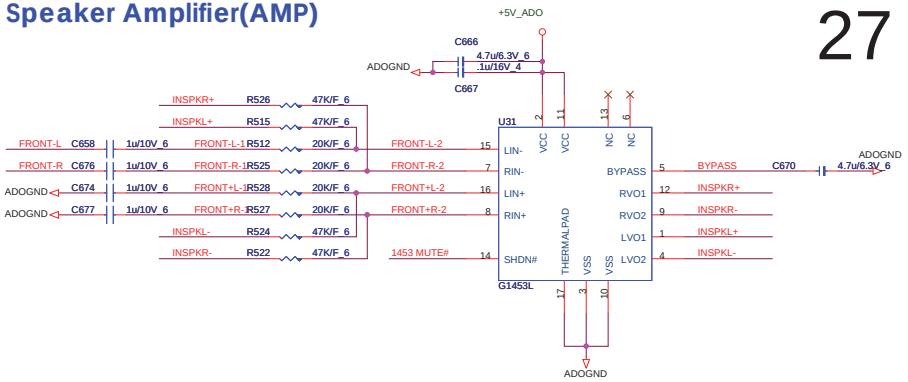
Codec CX20561-15Z (ADO) QFN



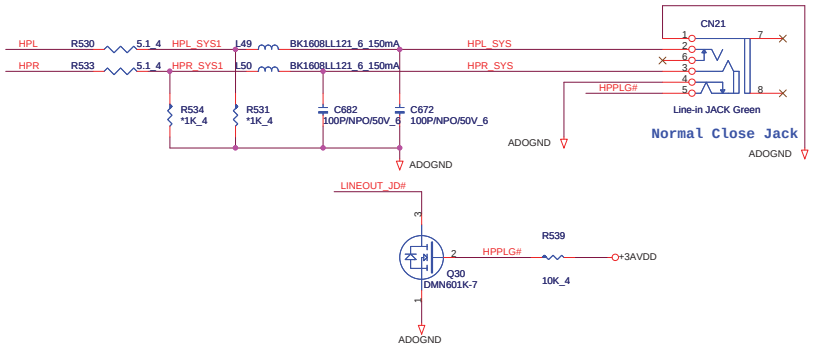
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

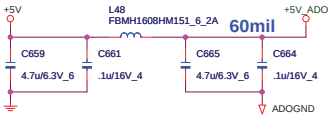
Speaker Amplifier(AMP)



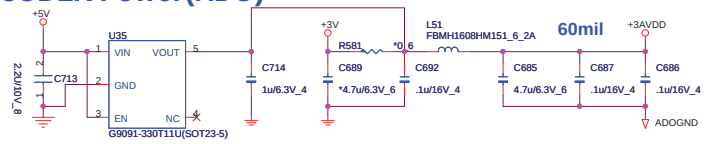
LINE OUT(AMP)



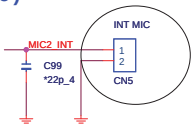
AMP Power(AMP)



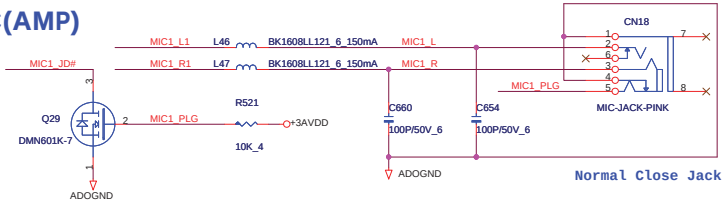
CODER Power(ADO)



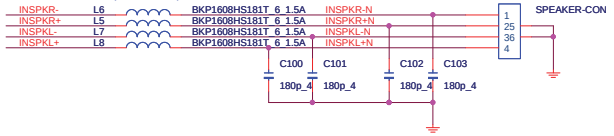
INT MIC.(ADO)



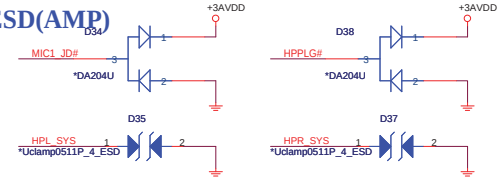
MIC(AMP)



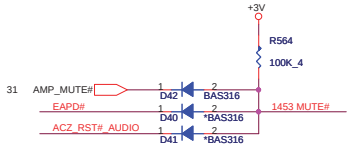
SPEAKER(AMP)



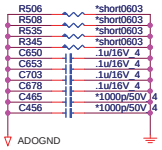
ESD(AMP)



MUTE(AMP)



(ADO)



Quanta Computer Inc.

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Size	Document Number	Rev
	CODEC/AMP/MDC	1A

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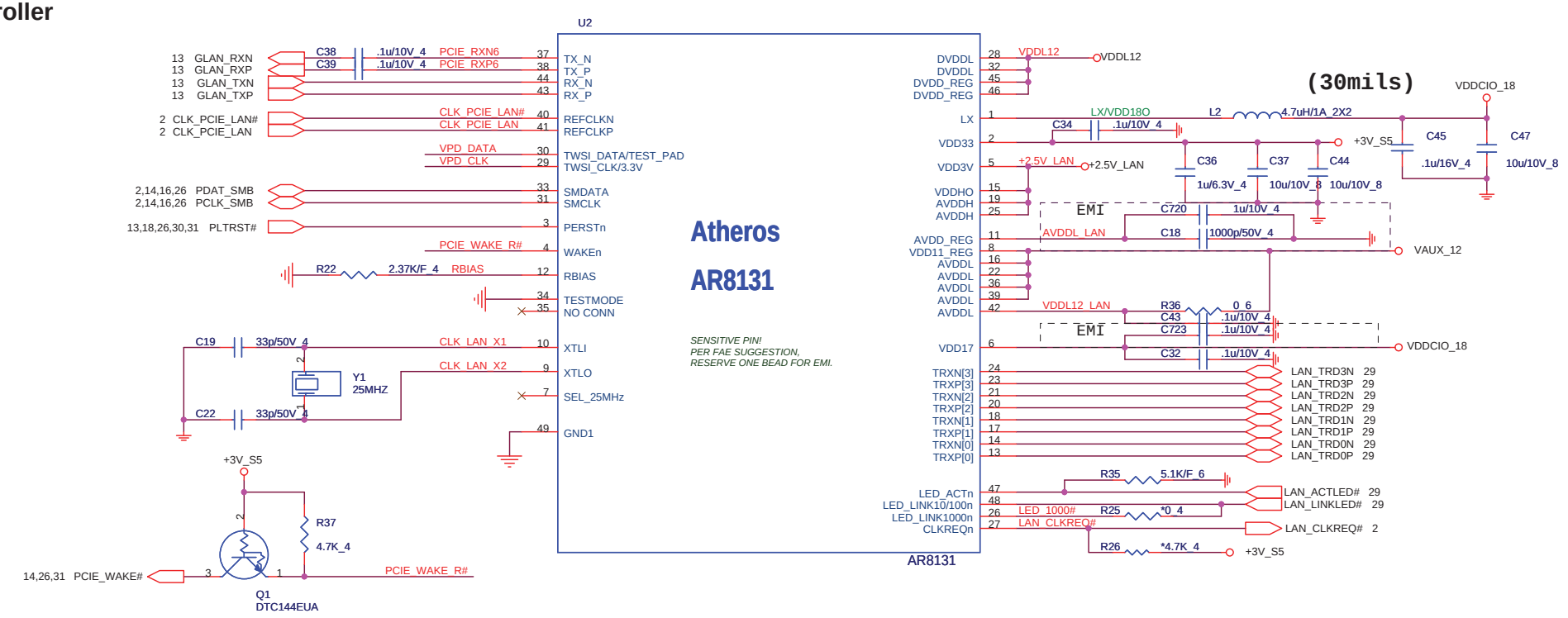
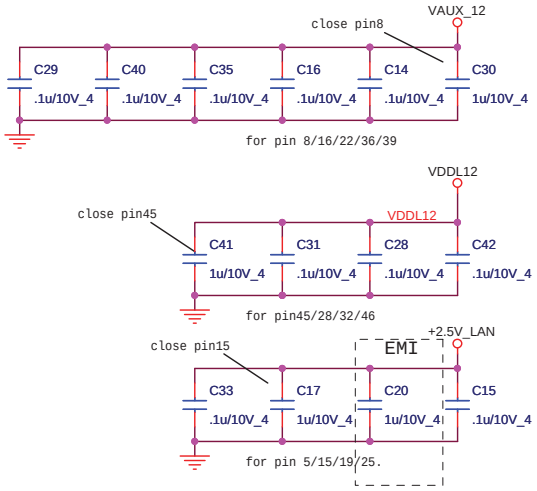
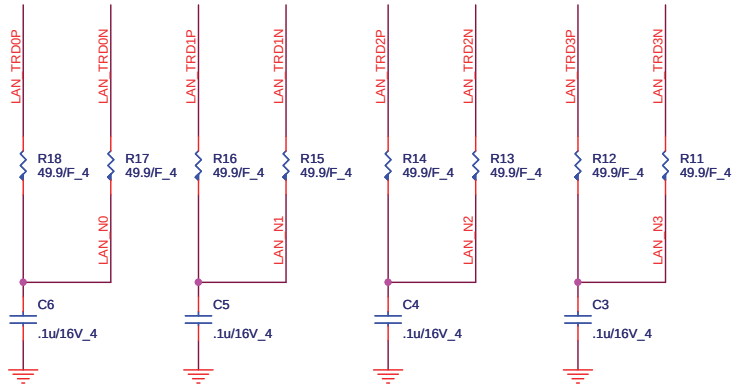
LAN Controller



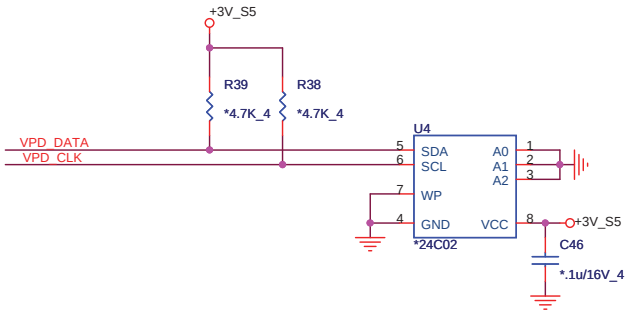
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	AR8131 GLAN	1A

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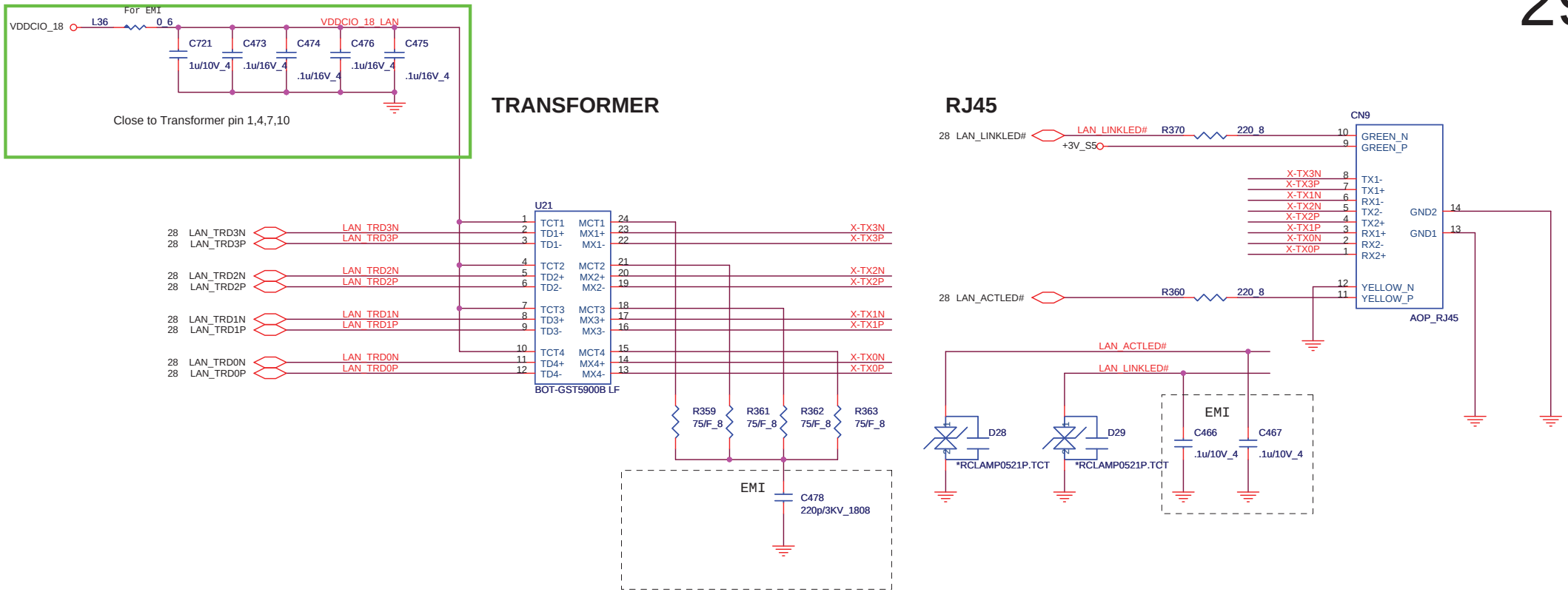

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	LAN Transformer and RJ45/BT	1A

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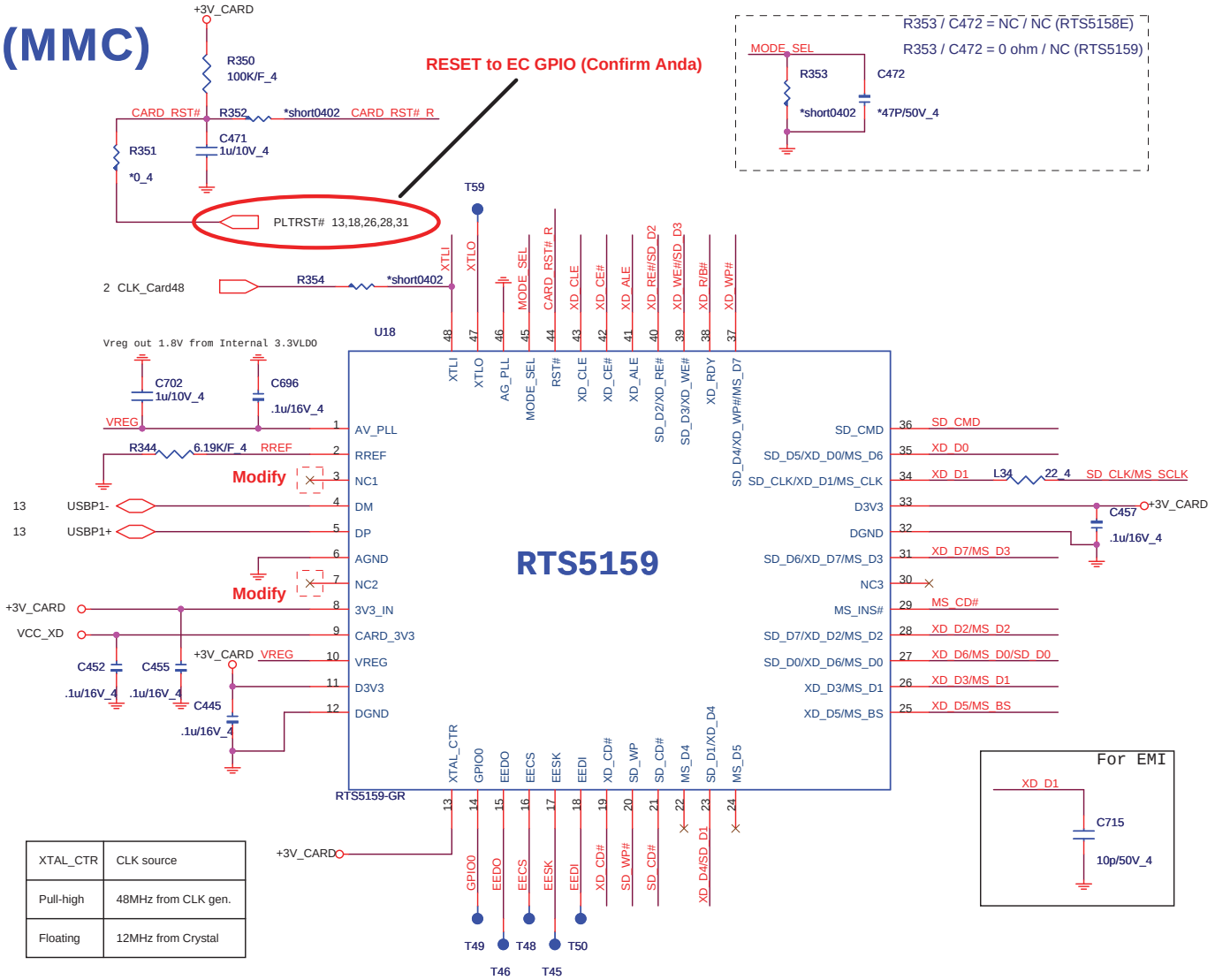
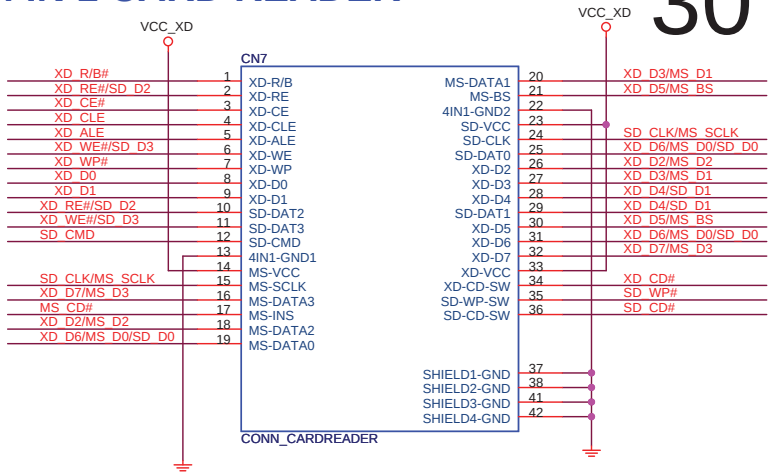
(MMC)

4 IN 1 CARD READER

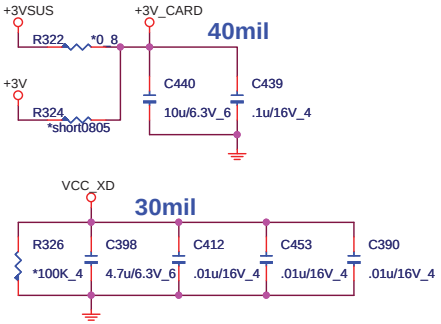
30



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal



CARDREADER POWER



Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	CARD READER RTS5159	1A

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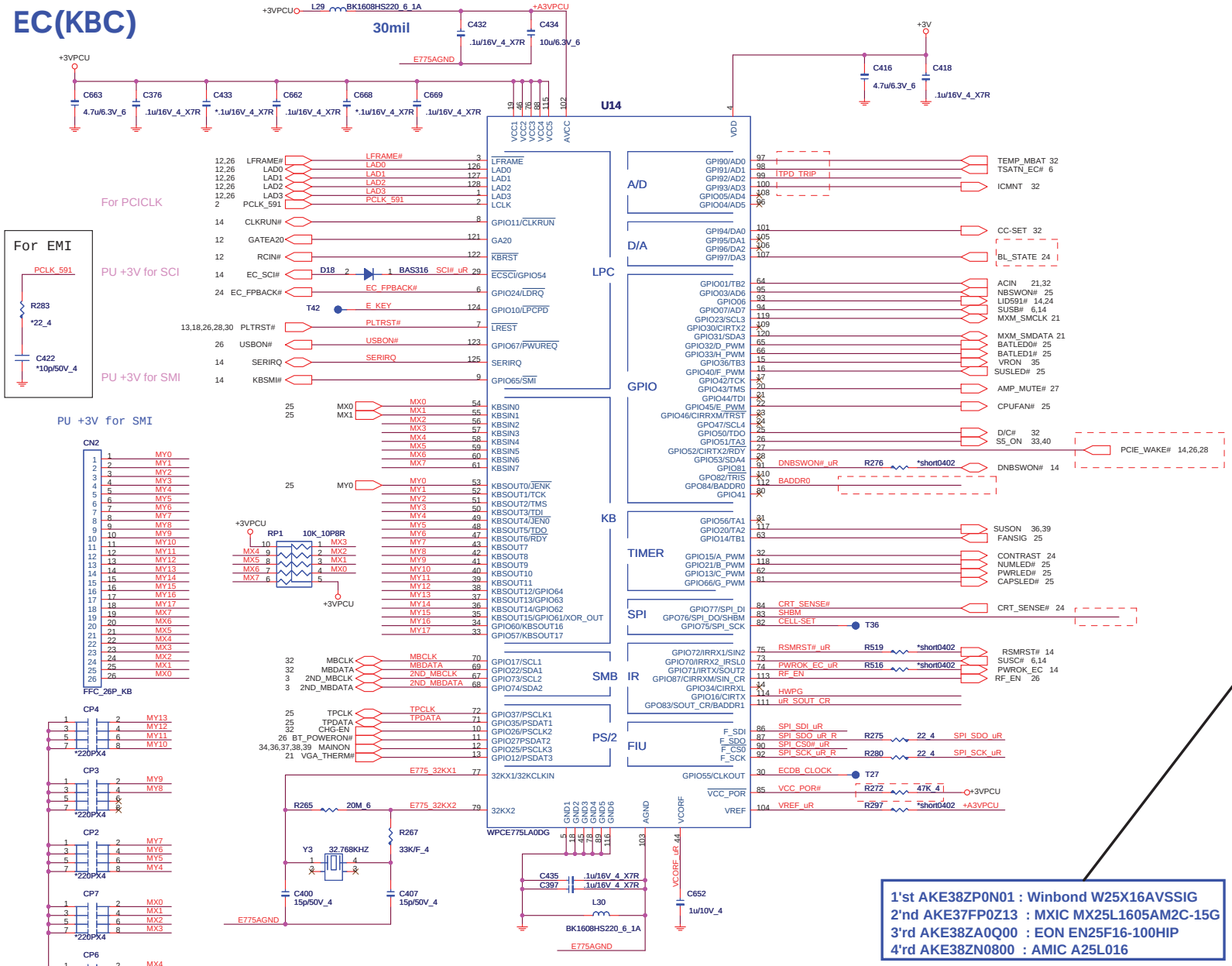
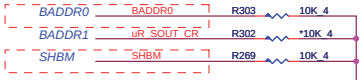
EC(KBC)



I/O ADDRESS SETTING

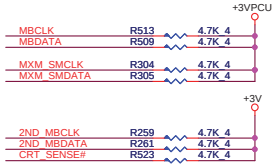
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

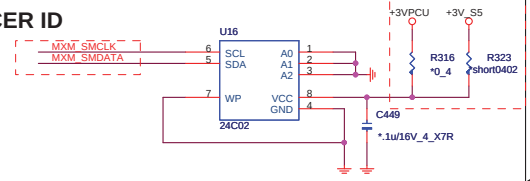


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

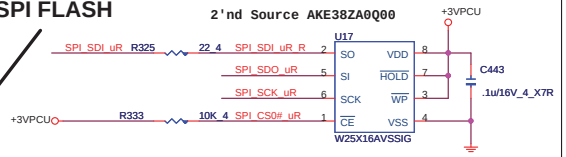


ACER ID



SPI FLASH

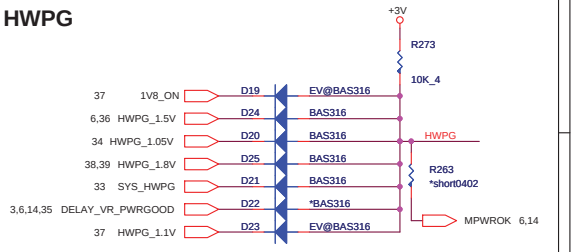
2'nd Source AKE38ZA0Q00



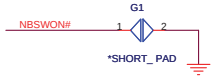
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

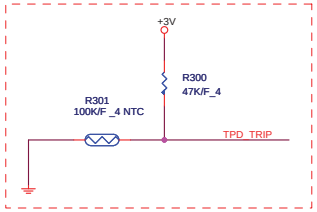
HWPG



POWER-ON PAD(UIF)



Thermal Sensor(THM)



INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.
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Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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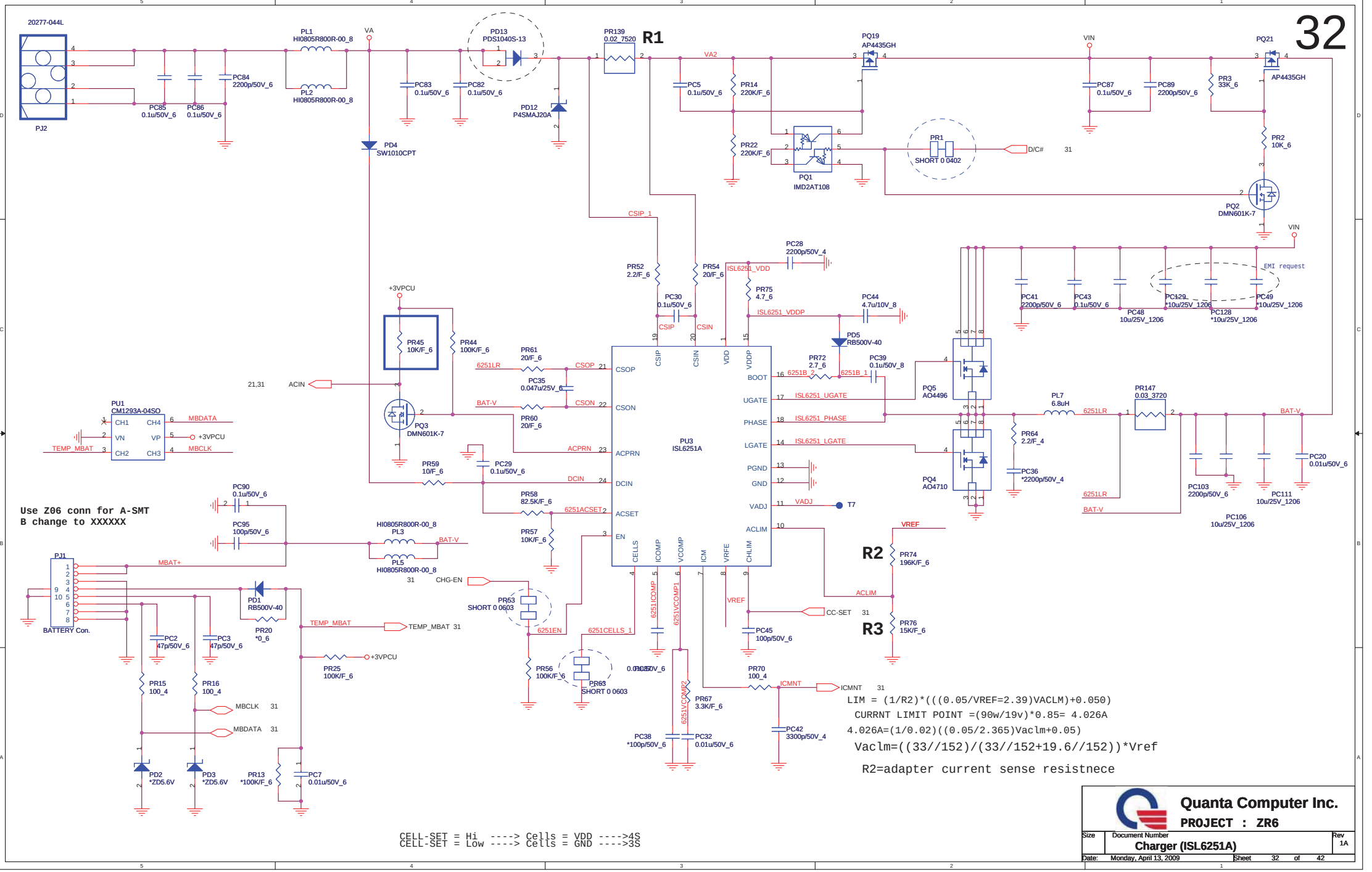

Use Z06 conn for A-SMT
B change to XXXXXX

LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece

CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

Quanta Computer Inc.			
PROJECT : ZR6			
Size	Document Number		Rev
	Charger (ISL6251A)		1A
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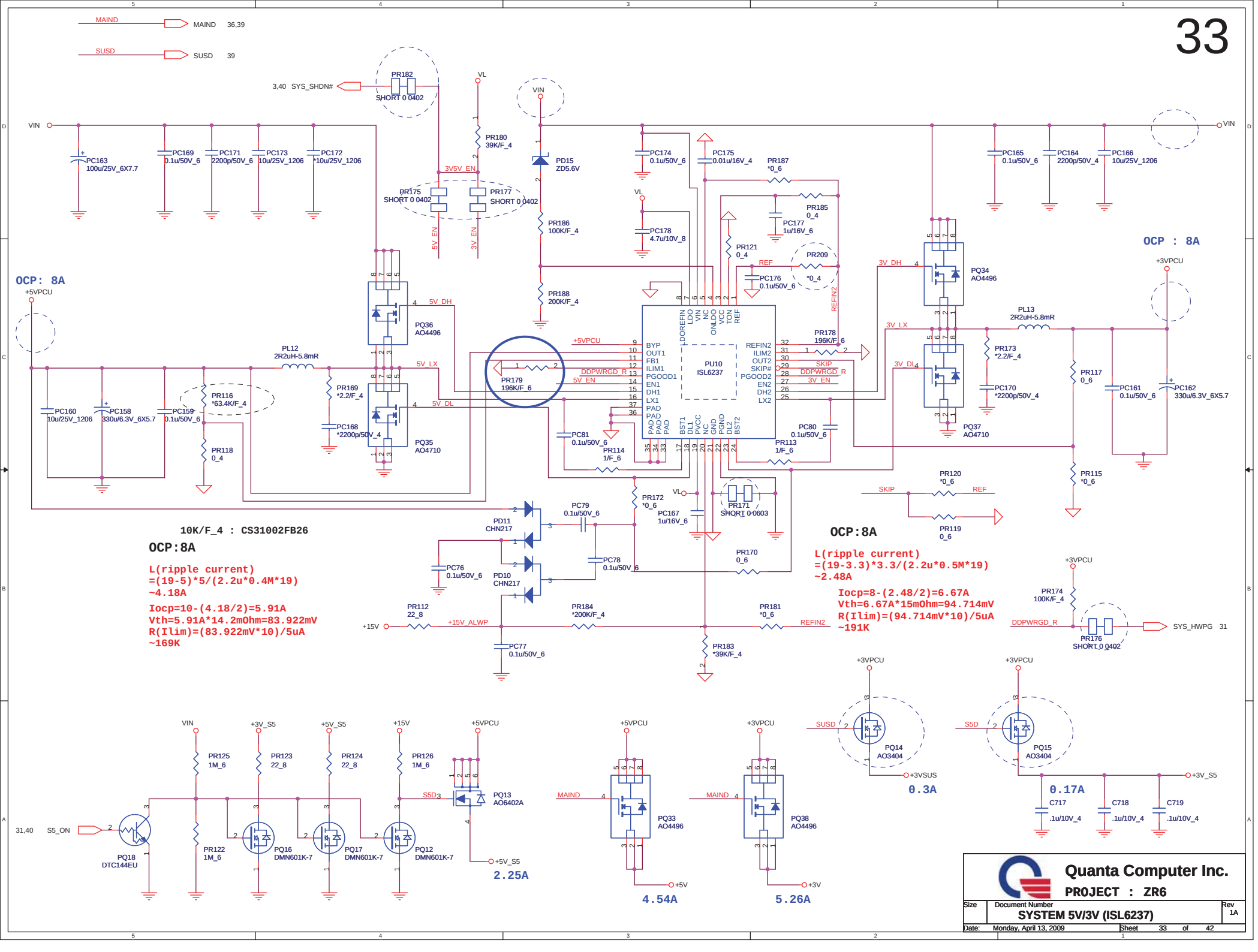

Quanta Computer Inc.

PROJECT : ZR6

Size	Document Number	Rev
	SYSTEM 5V/3V (ISL6237)	1A

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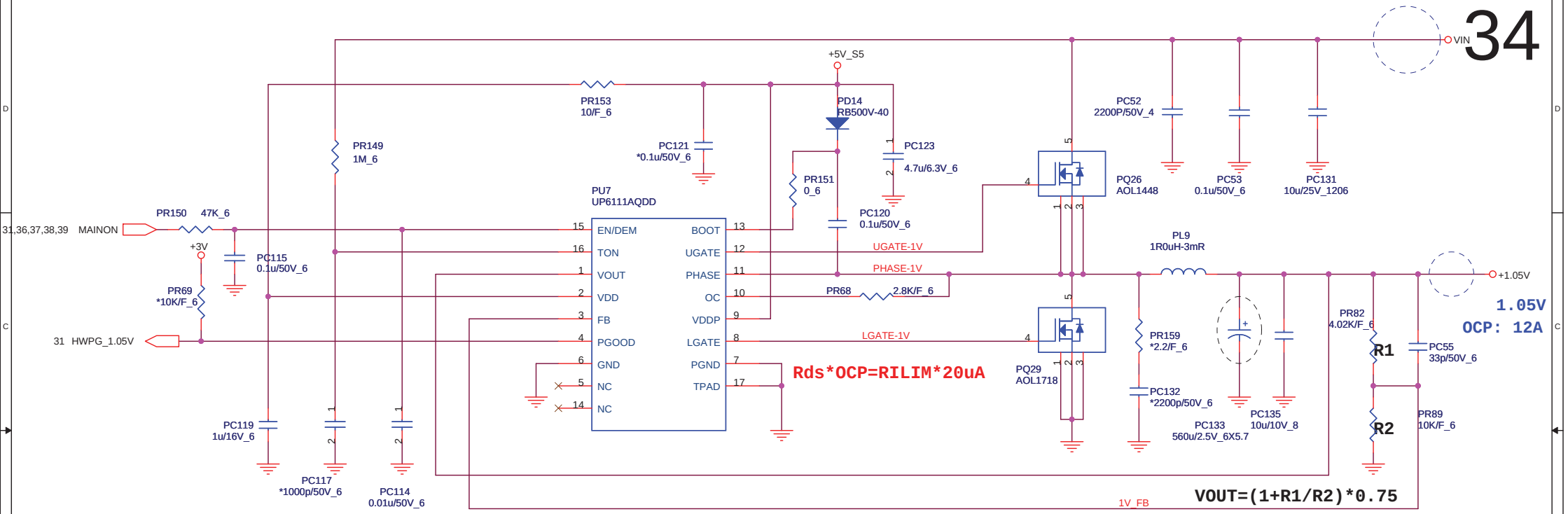


TON=3.85p*RTON*Vout/(Vin-0.5)

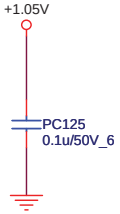
Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm
OCP=16-0.8A
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*12=RILIM*20uA
RILIM=2.76K--- 2.8K



Quanta Computer Inc.

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Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A

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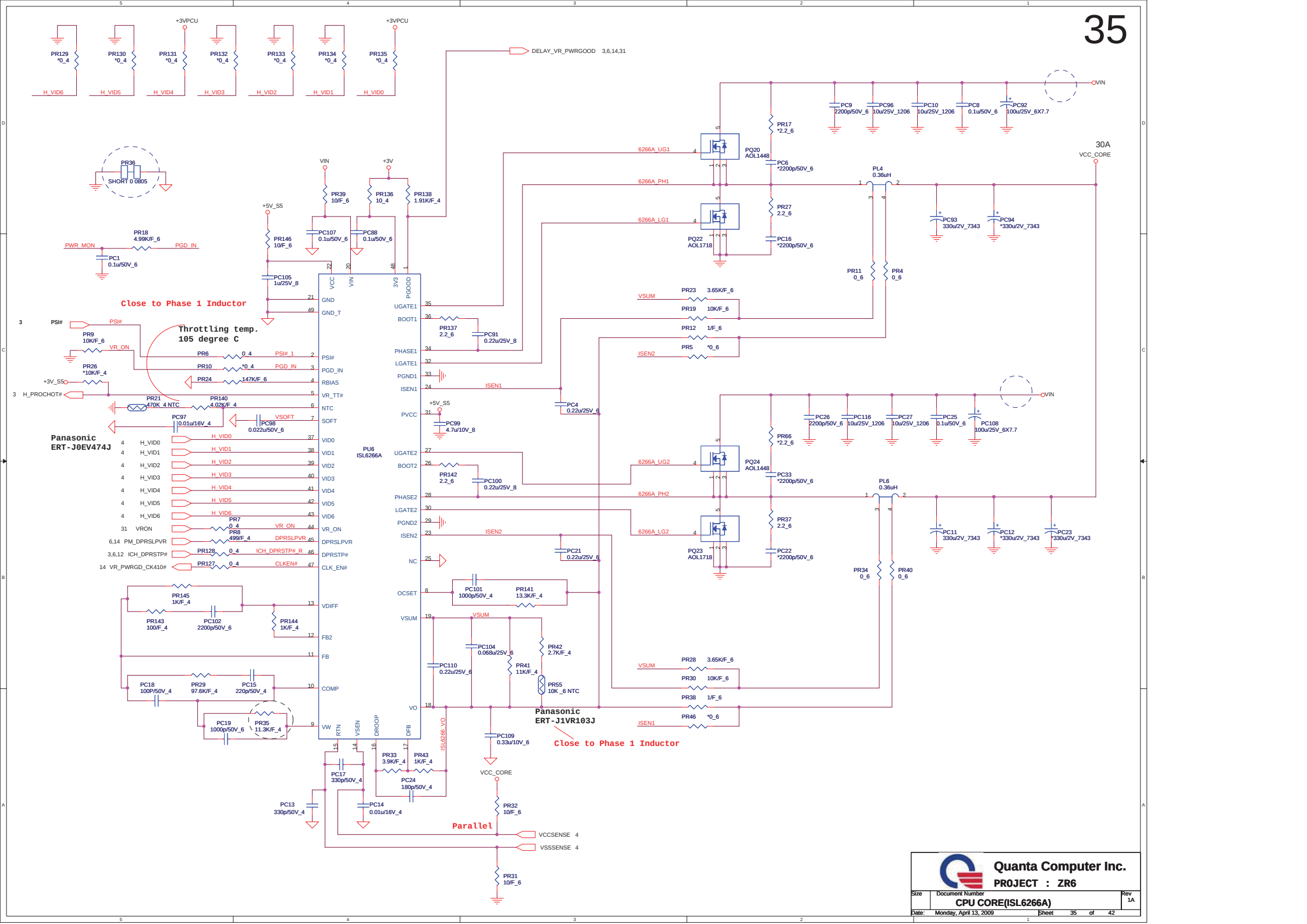

Quanta Computer Inc.

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Size	Document Number	Rev
	CPU CORE(ISL6266A)	1A

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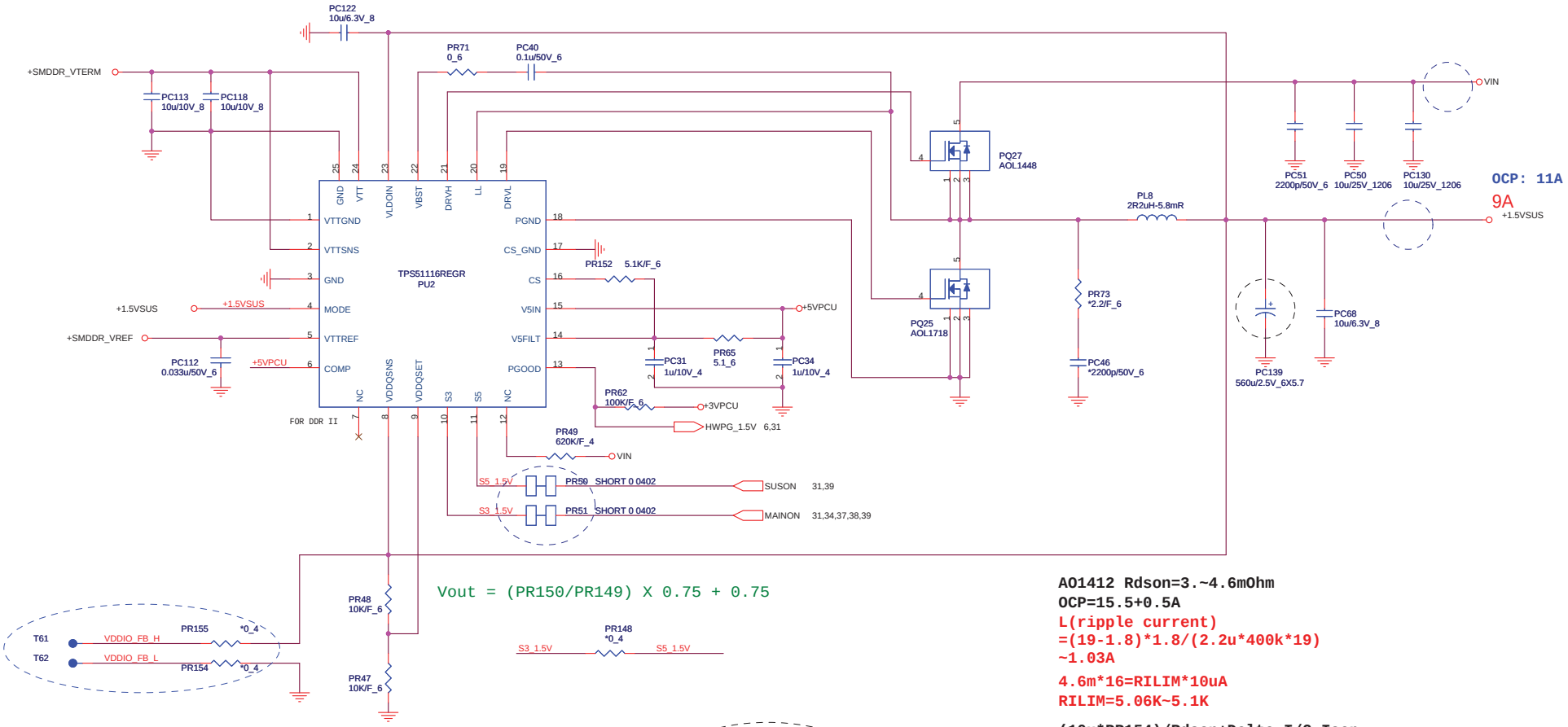

Vout = (PR150/PR149) X 0.75 + 0.75

AO1412 Rdson=3.~4.6mOhm
OCP=15.5+0.5A
L(ripple current)
=(19-1.8)*1.8/(2.2u*400k*19)
~1.03A

4.6m*16=RILIM*10uA
RILIM=5.06K~5.1K

(10u*PR154)/Rdson+Delta_I/2=Iocp

Quanta Computer Inc.
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Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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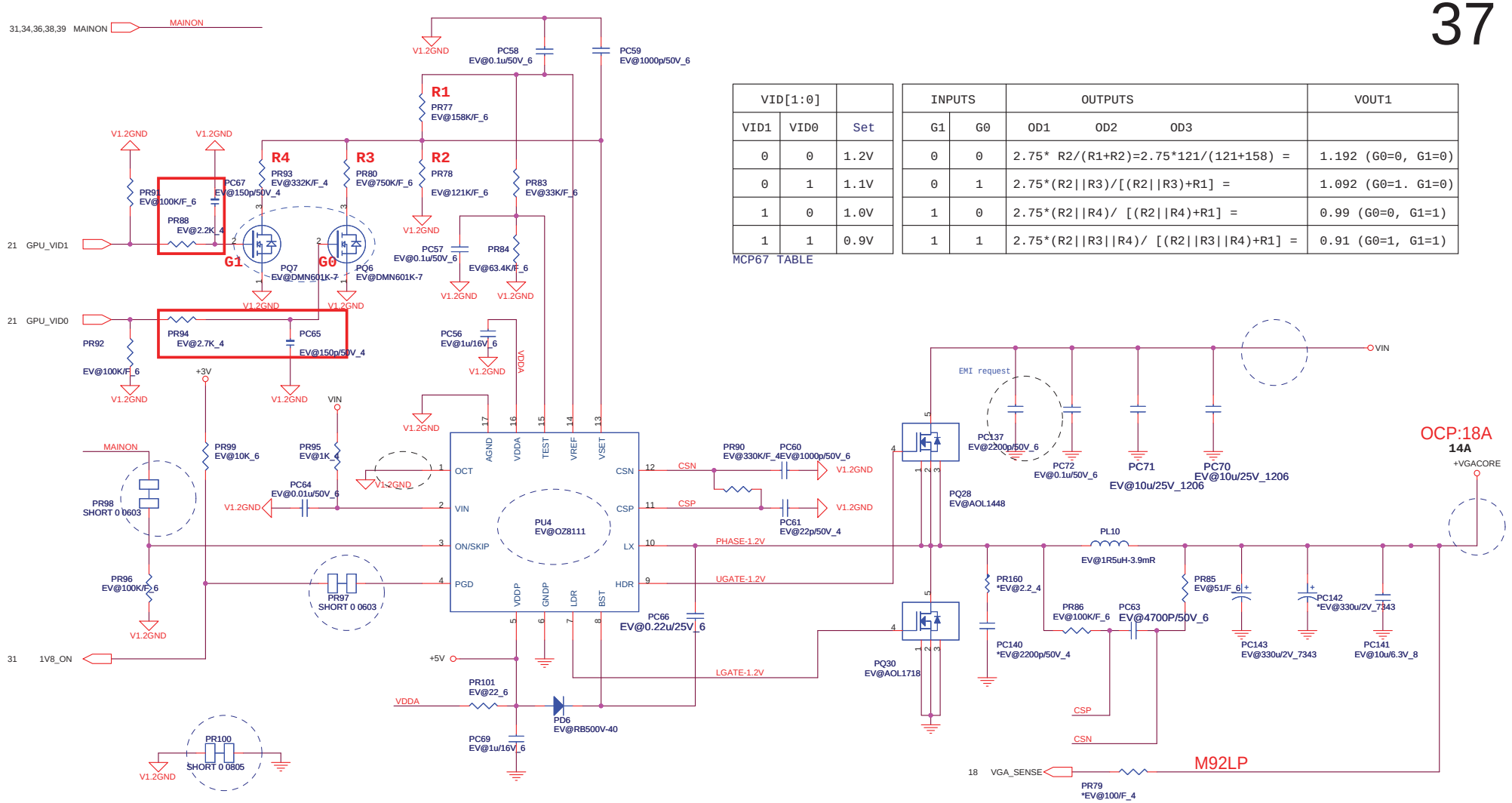

VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

MCP67 TABLE

INPUTS		OUTPUTS			VOUT1
G1	G0	OD1	OD2	OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =			1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =			1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =			0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =			0.91 (G0=1, G1=1)

Quanta Computer Inc.

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Size	Document Number	Rev
	VGA M92LP (OZ8118)	1A

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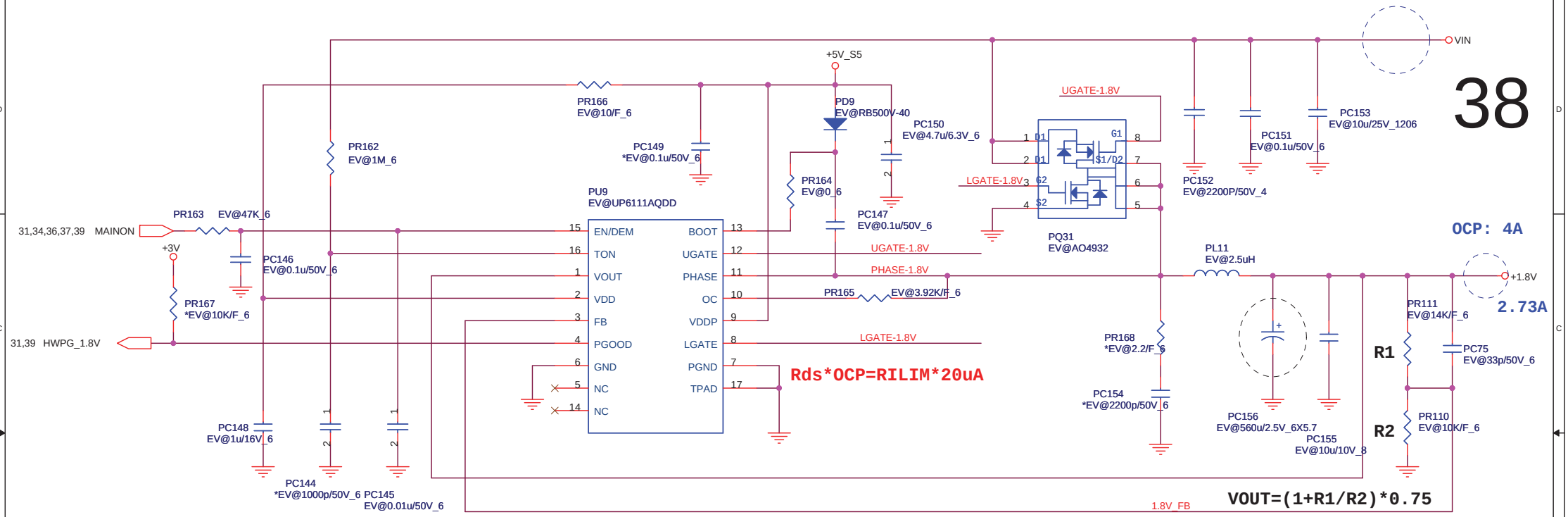

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4932 Rds=15.6~19.6mOhm
OCP=16-0.8A
L(ripple current)
=(19-1.8)*1.8/(2.5u*272k*19)
~2.14A

19.6m*4=RILIM*20uA
RILIM=3.92K

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Size	Document Number	Rev
	VCCP 1.8V(UP6111A)	1A

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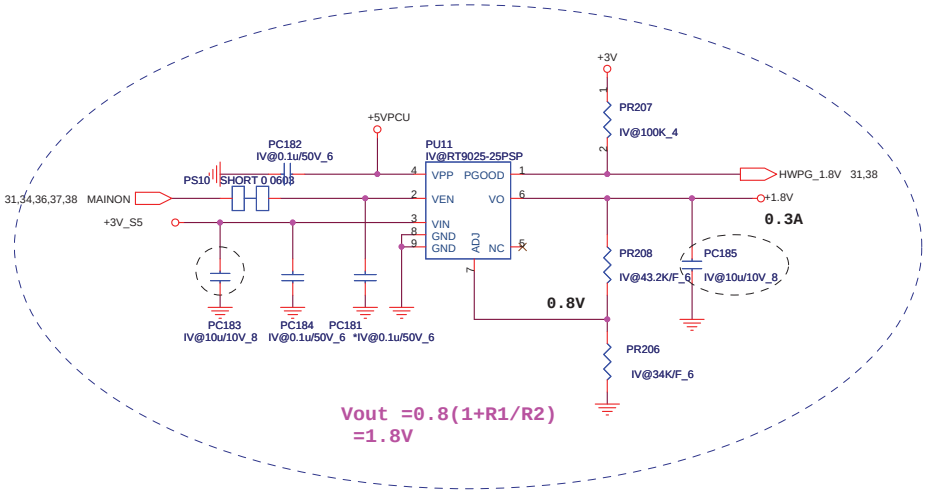

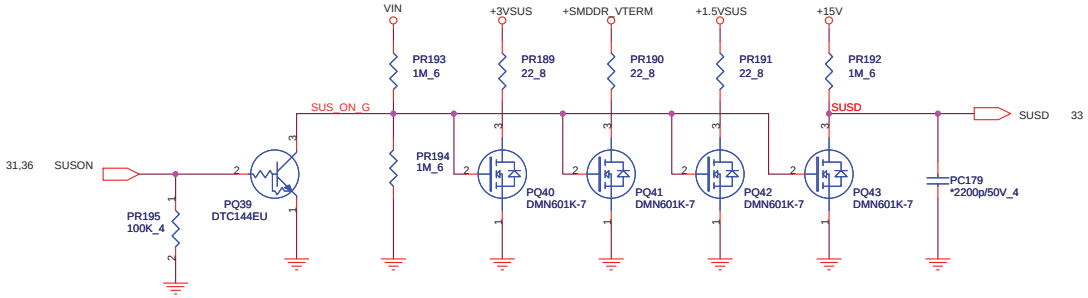

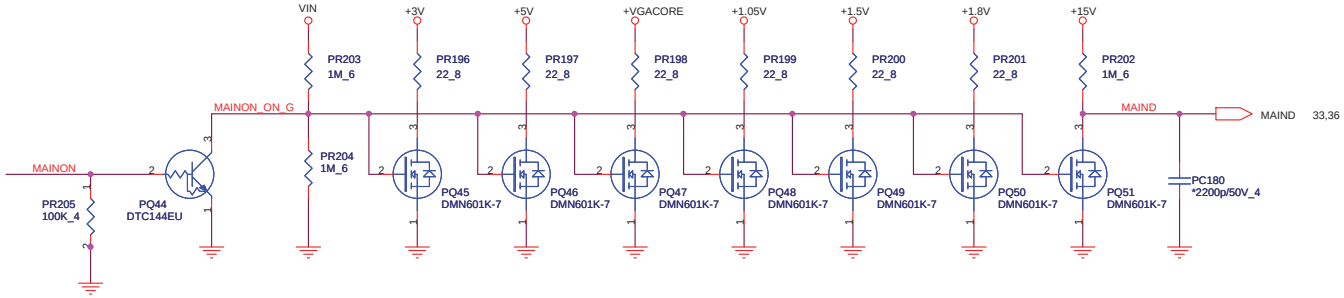

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	Discharge	1A

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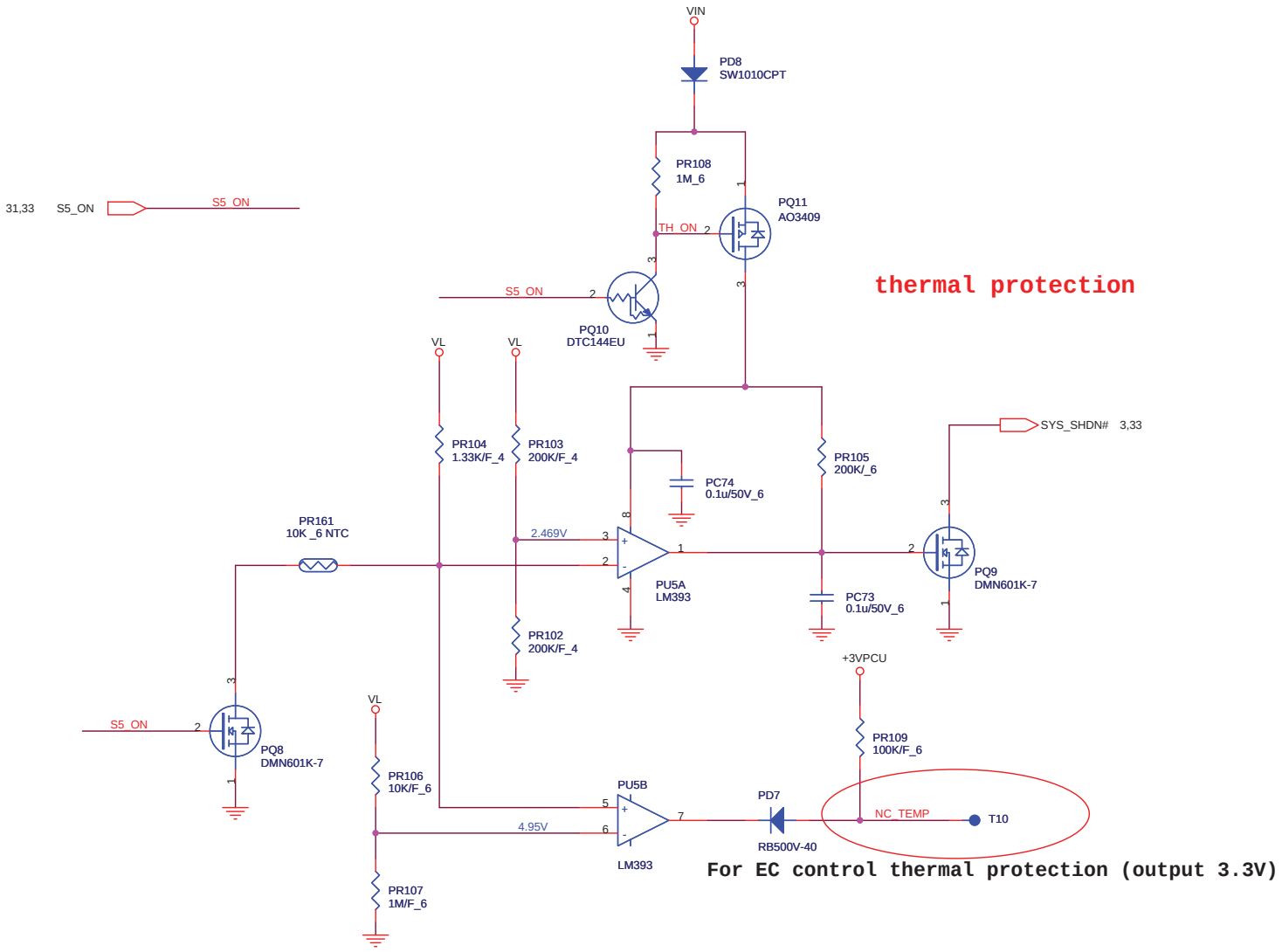

For EC control thermal protection (output 3.3V)

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Size	Document Number	Rev
	Thermal Protection	1A

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MODEL:	REV	CHANGE LIST
ZR6 MB	A	*First release*
	B	*Page23:Change C209,C522,C567,C533 from CH31003MB14 to CH41002KB93*
		Page10:change net name +1.8VSUS_TXLVDS-->+1.5VSUS_TXLVDS,+1.8VSUS_VCC_SM_CK-->+1.5VSUS_VCC_SM_CK
		Page24:change R174 from 100k to 470K,Del R177 to slove Hall sensor issue
		Page25:U12 No stuff and Del R248 to no stuff
		Page12:Change R543,R542,Q31 to no stuff,because ZR6 battery can't charging
		Page21:VGA ID pin R387 stuff 15k,R382 stuff 45.3K,R414 stuff 25K,R381/R415 no stuff
		Page14:MB ID pinR298 Value change to EV@,R308 Valule change to IV@
		Page26:change L25 layout and del RN19 and change L23 layout and del RN14
		Page24:change L1 layout and del RN1
		Page24:Change LCD connector(OT2)
		Page33:Mirror the PJ2 connector
		Page26:change CN19 footprint to mipci800055fb052g100pl-52p-ldv as ZG5 and Del debug card 0 ohm R518,R517,R514,R511,R510,R315,R310
		Page6:Change DD3 power OK circuit as ZK6
		Page26:Del R520,R529 and change R538,R536,R532 footprint to short pad
		Page24:U11 add pin 49 to thermal pad gnd
		Page25:Change CN3 footprint to af712l-a2g1t-12p-l-zr6
		Page32:Change CN2 footprint to 88502-260N-26P-L-ZR6
		Page29:Change U21 footprint to trf-10-1-24p-zr6
		Page27:Change U33 footprint to tqfn48-7x7-5-49p-zr6
		Page26:Change CN8 footprint to bl123-10r-10p-l-zr6
		Page25:Change D1、D2、D3 footprint to led-ht-110nb5-3p-zr6
		Page27:Change CN18 Part Number to DFTJ06FR212 and Change CN21 Part Number to DFTJ06FR211
		Page33:Change PJ1 Part Number to DFHD08MR064 for ZR6
		Page17:Change C502 to no stuff for cost down
		Page26:Change CN8 footprint to bl123-10r-10p-l-zr6& Partumber change to DFFC10FR017
		Page2:Del RN15,RN36,RN18,RN22,RN20,RN24,RN23 for cost down &Change R252,R244,R499 to short pad
		Page4:Change C58 to No stuff
		Page29:change R366,R367,R357,R358 to short pad for cost down
		Page27:change R506,R508,R535,R345 to short pad for cost down
		Page24:Del R346,R7 for cost down
		Page25:Del R218,R407 for cost down
		Page26:change C683,C675 to no stuff
		Page31:Add C715 for EMI
		Page31:Del C466,C467,L35 for cost down
		Page24:Add CN1 Pin33,Pin34 to GND ,Add R248,R218 for HDMI and Add L52,L53,L54,L55 for EMI
		Page10:change L38 to R037
		Page2:Add R511 for Mini_CLKREQ# pull up
		Page40:change +3VSUS to +3V_S5,HWPG_1.5V to HWPG_1.8V
		Page24:1.Del R248,R218,2.L19,L21 change to R218,R234,3.change D14,D15,R196,R197,R203,R200 vaule to stuff
		Page12:Change C450,C451 to 18P
		Page28:Change C19,C22 to 33P
		Page21:Add MXM ACIN circuit,R177R182,Q33,Q32,R183
		Page27:change R574 to no stuff and R541 to stuff
		Page24:Add D44 and Del R410
		Page28:change R39,R38,U4,C46 to no stuff
		Page18-23:change T65,T74,T11,T69,T68,T64,T67,T70,T73,T66,T72,T71 footprint to T3050
		Page26:Change C629 to 100uf and C636 to no stuff
		Page6:change R175 and R181 to 47K for HDMI vender request
		Page24:Change R197,R200 to EV@

MODEL / PAGE	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB0000/10/20/30/40/50/60/70	Project :ZR6 MB	Document No.:
Approved by : Johnny_O	Drawing by :Andy Chen	DATE: 2009/03/04

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MODEL:	REV	CHANGE LIST
ZR6 MB	B	Page6:change R175 and R181 to 4.7K for HDMI vender request
	C	Page10:change net name +1.5VSUS_TXLVDS--> +1.8V_TXLVDS Page3:Del Q5,Q6,R62,R63 Page3:change Par Number from AL000780000 to AL000780003 for thermal sensor address change to 9AH Page21:Del Q10,Q9,R96,R86 Page27:R574 stuff and R541 no stuff Page31:R300,R301 stuff thermal sensor Page37:change PC65,PC67 to 150pF Page28:change U2 PartNumber from AL008131001 to AL008131002(LAN chip) Page27:change R530,R533 from 10 ohm to 5.1 ohm for headphone Page27:change CN8 (usb) 12 pin board to board Page26:Change CN5 footprint to cwy027-b0g1z-2p-l,CN16(USB)footprint change to usb-c107h6-10405-l-4p-r-v-nb4 Page30:Change CN7 footprint to 4IN1-R015-212-LM-42P-H-nb4 Page32:PJ1 footprint change to bat-btj-08qn0b-8p-r-v-nb4 Page32:Del R510,change Hole15 footprint from h-tc315bc433d106p2 to h-tc315bsd106p2 Page04:change C493 to no stuff Page27:Del T77 and Add R62 Page26:change Hole21 footprint to h-c236d142pt-8 Page24:Change D1、D2、D3 footprint to led-ht-110nb5-3p Page24:Change R218,R234 to shortpad Page26:Change R310 to shortpad Page10:Change R91,R307,R418,R466,R469 to shortpad Page29:Add C466,C467 for EMI,Add R358,R357,R366,R367 and change DGND to LAN GND Page26:Add C716 for EMI Page30:Change L34 to 0 ohm and C715 to 10P,Change R512,R525,R528,R527 to 20K 1% and Change R526,R515,R524,R522 to 47K 1% Page25:Change R1,R4,R10,R365,R369,R368 to 221 ohm and Change D1,D2,D3 part number Page14:Change R282 to no stuff Page28:Change R26 to no stuff Page26:Change Hole29 part number to MBZR6005010 Page29:Del net name LAN_LNK_LED_PWR
	D	Page14:Add R583 and R315 at GPIO7 for HDMI option,change R583 to no stuff and R315 to stuff Page24:change HDMI item to no stuff(remove this function) Page12:change R225,R216,R241,R220,R219,R215,R213,R214,R228,R227 to no stuff for remove HDMI Audio Page26:Change Hole 16 footprint as hole1
	E	Page37:change PR97,PR98 to short-pad ,change PU4 OZ8116 change to OZ8111 for cost issue ,Del PC62 Page27:C670 change value from 1U to 4.7U (CH5471M9907) Page29:change c478 from 1000p to 220p.(CH122GK1I10) Page28:change C18 from 0.1u to 1000p (CH21006JB10),change C20 from 0.1u to 1u (CH5102K9B06) ,ADD C723 0.1u (CH41002KB93),ADD C720 1u (CH5102K9B06) Page25:change DHP00DA1G03->DHPTME53201 Page24:add C722 (CH6101M9905) to solve ISN issue Page27:the PC beep will change Gain from -6db to -18 db , so R559 needs stuff 10k on all BOM. Page34:change PC133 from CC7560JMZ15 to CC7560JMZ02 for cost down Page36:change PC139 from CC7560JMZ15 to CC7560JMZ02 for cost down Page38:change PC156 from CC7560JMZ15 to CC7560JMZ02 for cost down Page33:change PC158,PC162 from CC73301MZB2 to CC73301MZ04 for cost down Page37:change PQ6,PQ7 from BAM700200F6 to BAM601K0003 for cost down

MODEL / PAGE	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
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31	3A	
32	2A	
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36	2A	
37	2A	
38	2A	
39	3A	3B
40		

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	Thermal Protection	1A

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